

The image features a vibrant red background adorned with numerous white snowflakes of various sizes and intricate patterns. At the bottom, a row of white silhouettes depicts a group of people in various dynamic poses, suggesting a lively dance or party atmosphere. A semi-transparent white horizontal band is positioned across the lower portion of the image, containing the text.

EED Holiday Party
-A year in Review-

EED Infrastructure Group Team: Steve Chappa, Walter Jaskierny, Dave Featherston, Arnab Ghosh, Tyler Griffin



This year, a lot of work involved rebuilding the Muon g-2 kicker electronic equipment racks

One of the three capacitor chassis, used by the Muon g-2 kicker system, that has been refurbished.



Again, lots of equipment and installation ORC (Operational Readiness Clearance) reviews...is this safe to operate?



Attempted revival of an old beamline magnet called the Jolly Green Giant and its power supply



Electrical Safety is always a concern...

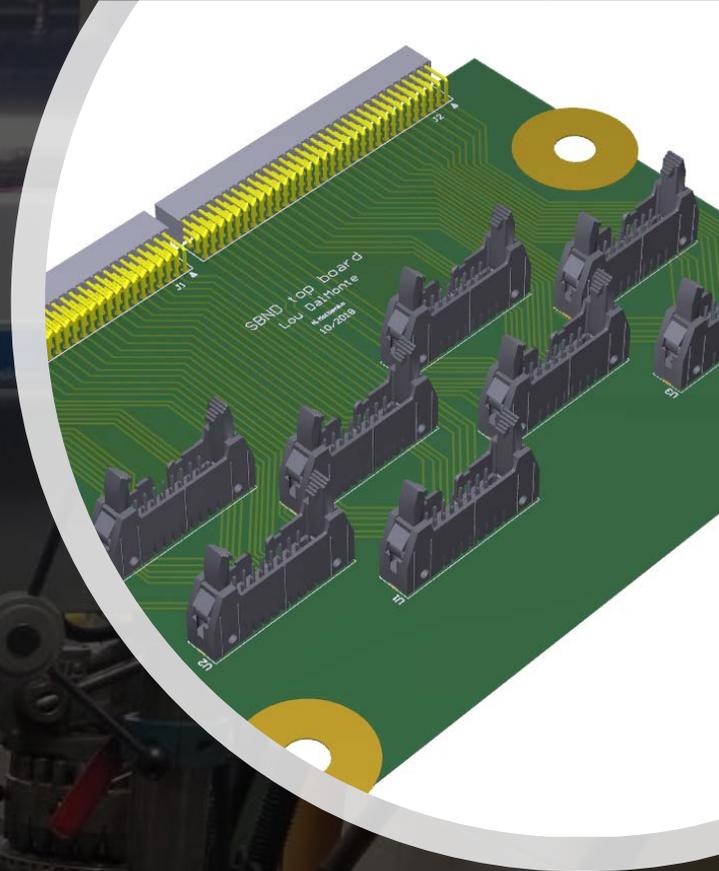


...and of course, all the new and updated electrical distribution installation that is required to power all this equipment



A relatively new addition to our task list: support and testing of large UPS systems. This one, used by SCDMS at SNOLAB, can supply up to 240 kW.





Paula, Nina, Curtis, Johnny, Victor

Infrastructure support

WHGF tech shop
Assembly Lab
PCB reworking
PCB layout

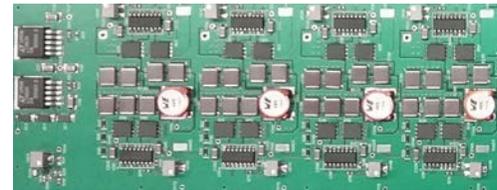
CAD support/Parts libraries
PCB Fabrication
Procurement management
Project management support

Projects for the Year

- Dave Huffman
- Mu2e Rack Protection
 - Dual AC Switch Box
 - Rack Protection System Chassis
 - Slow Controls



- Tracker Low Voltage
 - Switched Capacitor Converter

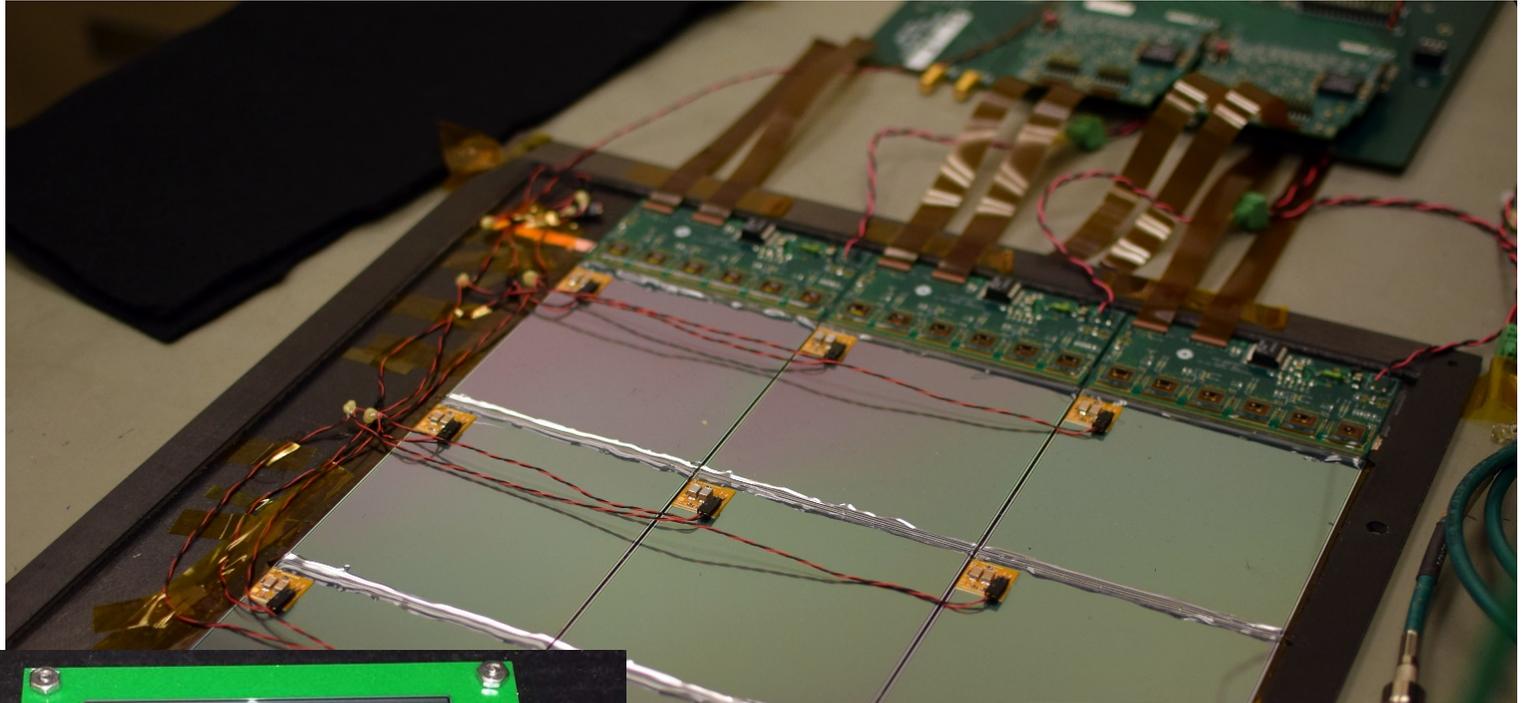


- Mike Cherry – Vacuum Vessel De-Magnetizing, ANNIE Support
- Tim Cunneen – Site wide Cameras and emergency alarms systems



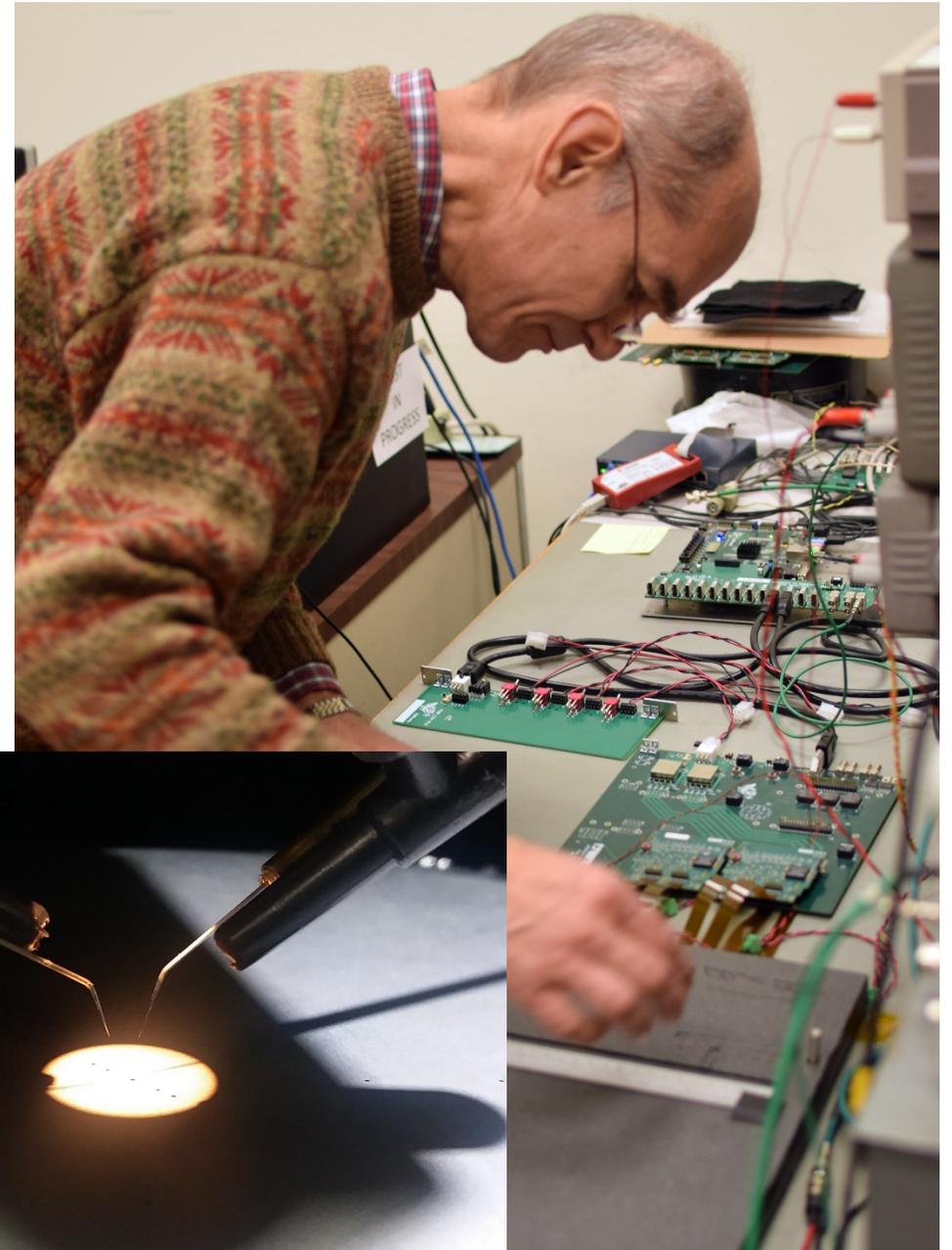
Mike Utes

- Silicon Muon Scanner with Ron Lipton, Andrew Green, Cristian
 - R&D100 Award Winning Project
 - Next phase installation at Nevada National Security Site
- Radioactive gas analysis project with Eric Church @ PNNL
 - Based on SKIROC2A ASICs used on the Silicon Muon Scanner
 - Detectors reading out cosmics
- Silicon strip monitor system for MTEST
- NIM Plus – modern NIM module where each channel can have a programmable pulse width and delay
- Impedance Monitor installation and commissioning used for Mu2e, Icarus, and Protodune
- Deputy Chair, Electrical Safety Subcommittee



Cristian Gingu

- Silicon Muon Scanner firmware and readout software
 - R&D100 Award
- CMS High Granularity Calorimeter (HGC) firmware
 - ECON concentrator ASIC emulation/testing
 - Xilinx Ultrascale+ ZYNQ FPA
- Radioactive gas analysis project with Mike Utes and Eric Church @ PNNL
- PHENIX experiment (BNL) Silicon Forward Tracker.
- VIPIC ASIC wafer level testing (ANL)
- Quantum Dots sensor measurements
- Broadband spectral sensitive graphene structures
 - Photodetectors / GFET transistors
 - LDRD project with Vadim



Kevin Kuk

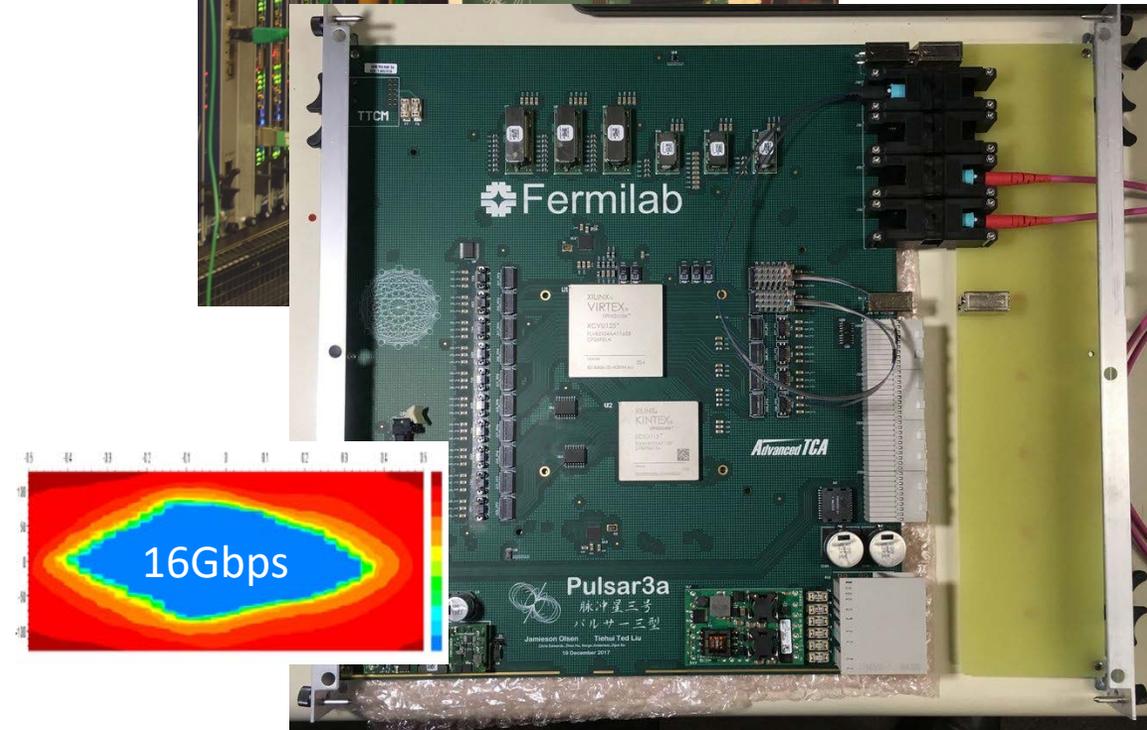
- Working on many different CCD-based experiments with Juan Estrada @ Sidet
- CCD based detectors for ultra cold neutrinos at LANL
- Building, testing, characterizing CCDs for the DESI instrument.
 - DAMIC, CONNIE, SENSEI
- Microwave Kinetic Inductance Detectors (MKIDs) readout and characterization
- Building a new multiCCD test chamber using a SunPower cryocooler for Skipper CCD production.
- Support of detector installation and fabrication at the SBN-ND.



Kevin with the ADR Cryo (Adiabatic Demagnetization Refrigerator) test stand in one of the SiDet clean rooms.

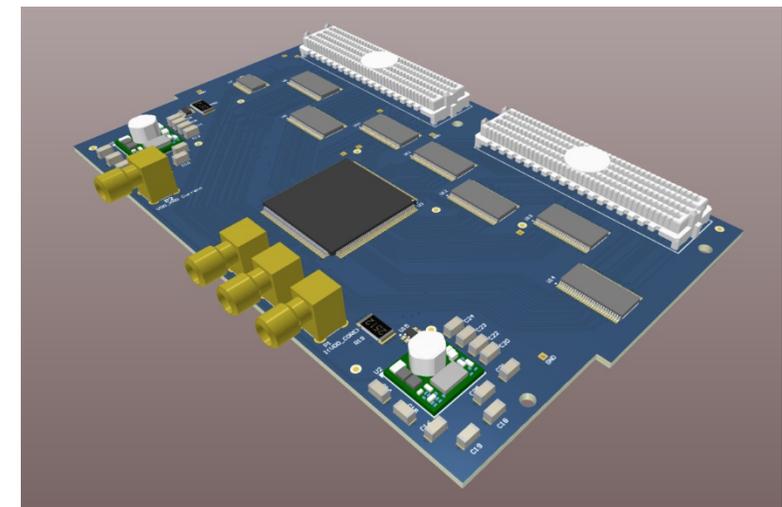
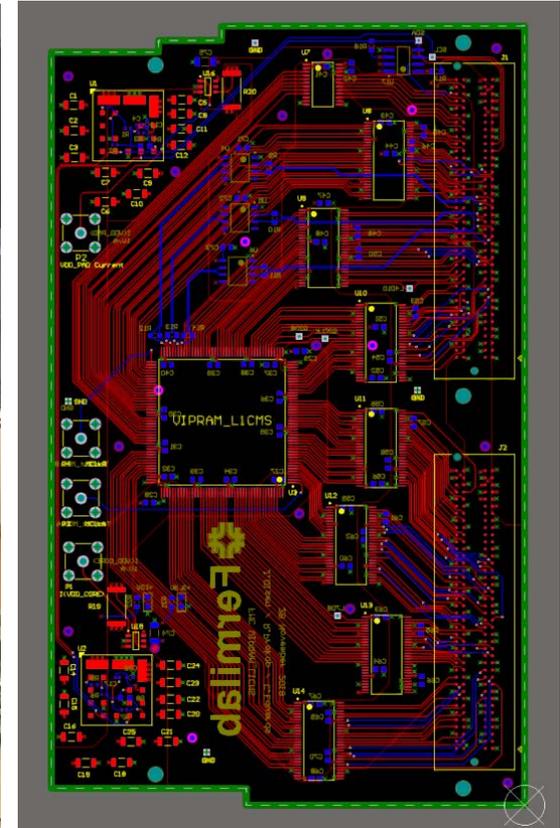
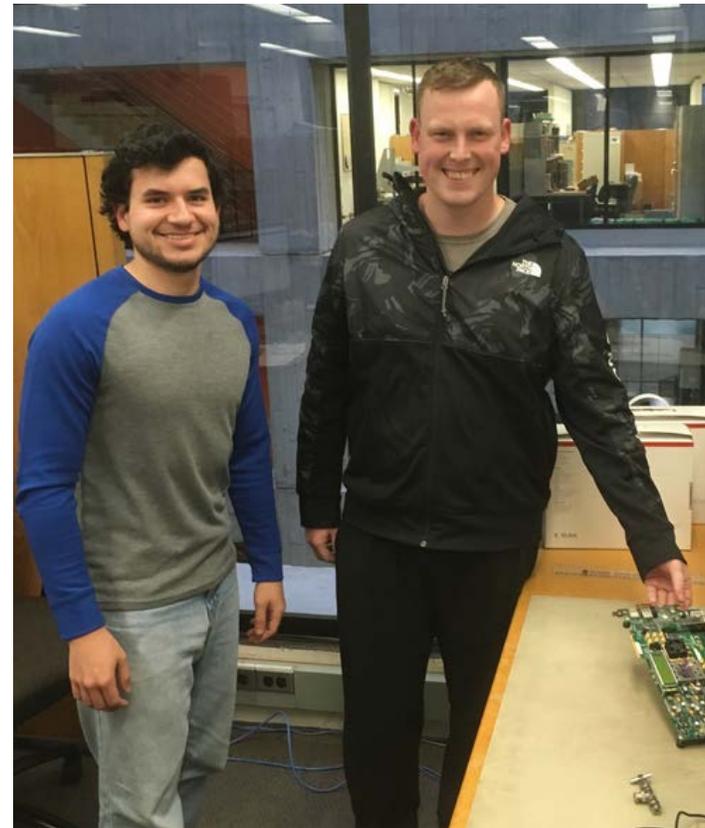
Jamieson Olsen

- 3rd Generation ATCA Pulsar board
 - Big FPGAs for track finding / pattern recognition
 - High speed optical and copper backplane links
 - L1 CMS Tracking Trigger R&D, PET imaging, etc.
- CMS Endcap Timing Layer R&D
 - LOTS of channels 30ps timing resolution
 - Clock distribution within new ASIC
 - Clock distribution at system/board/crate level
- CMS ECON concentrator ASIC
 - ASIC test/characterization and emulation in FPGA
- Getting ready for VIPRAM_L1CMS ASIC testing with Co-Ops
- Detector Electronics Group Leader
- Supervising two Co-Op students
- Co-Chair, Engineering Promotion Committee



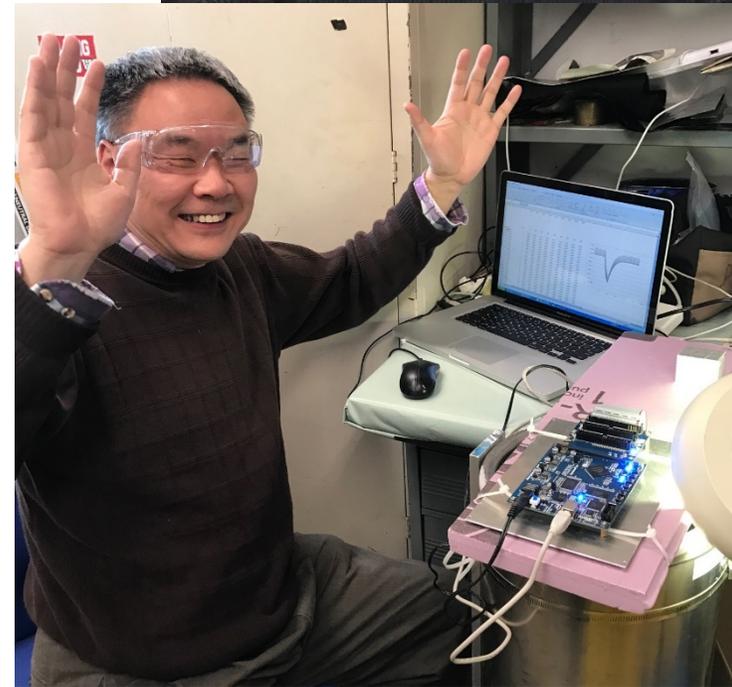
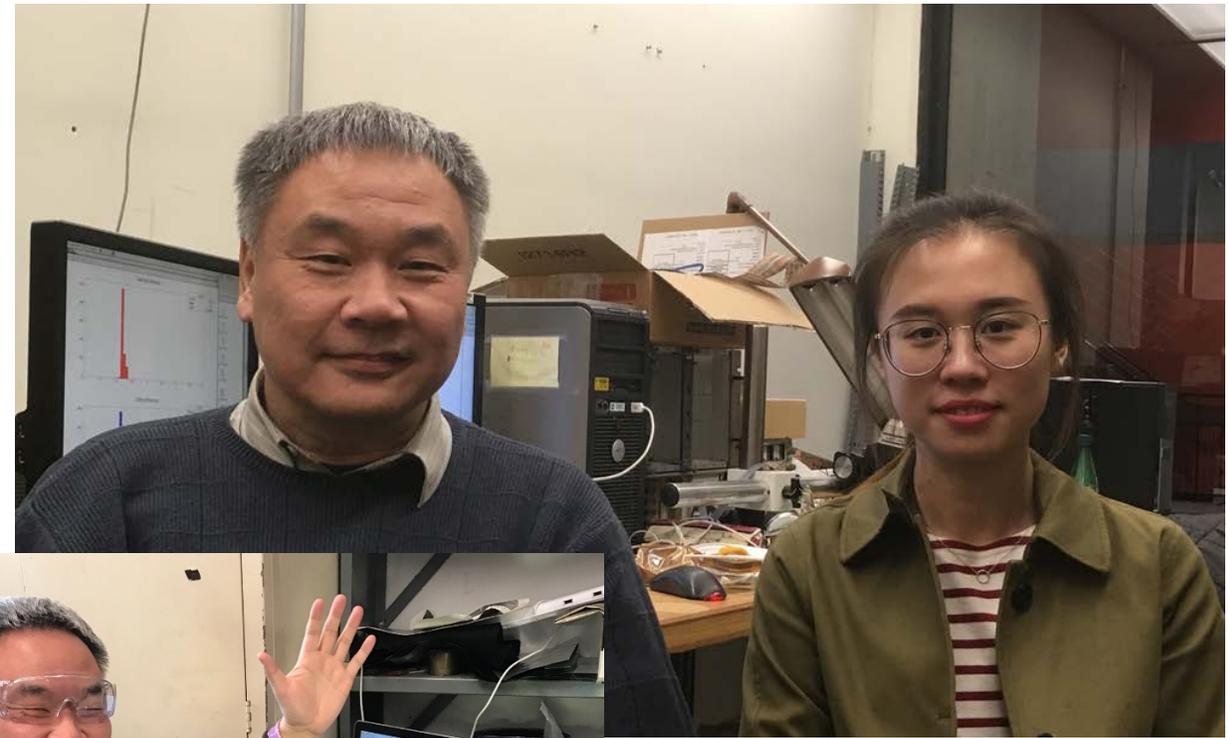
Co-Op Students

- Chris Edwards
 - NIU BSEE August 2019
 - 3rd and final co-op term!
 - Firmware design and simulation for testing VIPRAM_L1CMS ASIC
- Rich Prokop
 - NIU BSEE May 2019
 - 3rd and final co-op term!
 - Designed Schematics and PCB Layout for VIPRAM_L1CMS ASIC test board



Jin-Yuan Wu and Jingjing Xu

- Jingjing Xu
 - Purdue University
 - Summer + Fall Semester 2018
- Precision time to digital (TDC) measurements in FPGAs.
 - Convert from older Altera FPGAs to modern Xilinx FPGAs
 - MAX+PLUS schematics to VHDL
 - FPGAs were never intended to do this!
- CMS Endcap Timing Layer R&D
 - Time of flight, Time over threshold measurements with picosecond accuracy
 - System level timing calibration



Sergey Los

- CMS HCAL Phase 1 upgrade
 - Production of signal and BV flex cables, SiPM mounting boards, and misc. hardware
 - Investigation/troubleshooting control board issues
- CMS phase 2 upgrade High Granularity Calorimeter (HGC) and OT (outer tracker) R&D work
 - Probe cards and various test boards
- Precision timing includes boards for LGAD sensors and SiPMs
 - CMS Endcap Timing Layer (ETL) readout and front end power distribution
 - Hardware in use at Fermilab Test Beam Facility (FTBF)



Sten Hansen and Terry Kiper

- Mu2e Cosmic Ray Veto
 - Front end electronics
 - Passed construction readiness review in August
 - 340 64-channel front end boards
 - 14 24-port readout controllers
 - Vertical slice test
 - Sten = Firmware
 - Terry = Microcontroller code
 - Both = schematics and layout
- CDMS warm electronics
 - 16 channel Detector Readout and Control Cards (DCRS) in production
 - Vacuum interface boards PCB layout by Nina
- Linac BPM modules modified for laser chopped/notched beam



New Arrivals in January 2019



- Miguel Marchan
 - Former GEM student
 - Starting as Engineer (E1) mid-January
 - Build up expertise in low noise analog front end design
- Gary Drake
 - Shorter commute!



ProtoDUNE Experiment at CERN



Contributions include following PPD/EED group members:
Terri Shaw, Paul Rubinov, Mike Utes, Steve Chappa, Arnab Ghosh, Lee Scott, Johnny Green and Brian Hess.

Provided systems integration (T. Shaw) for the ProtoDUNE experiment.

Detector makes use of “Isolated” detector ground and AC distribution designed at FNAL and implemented at CERN. Ground Impedance Monitor provided by FNAL.





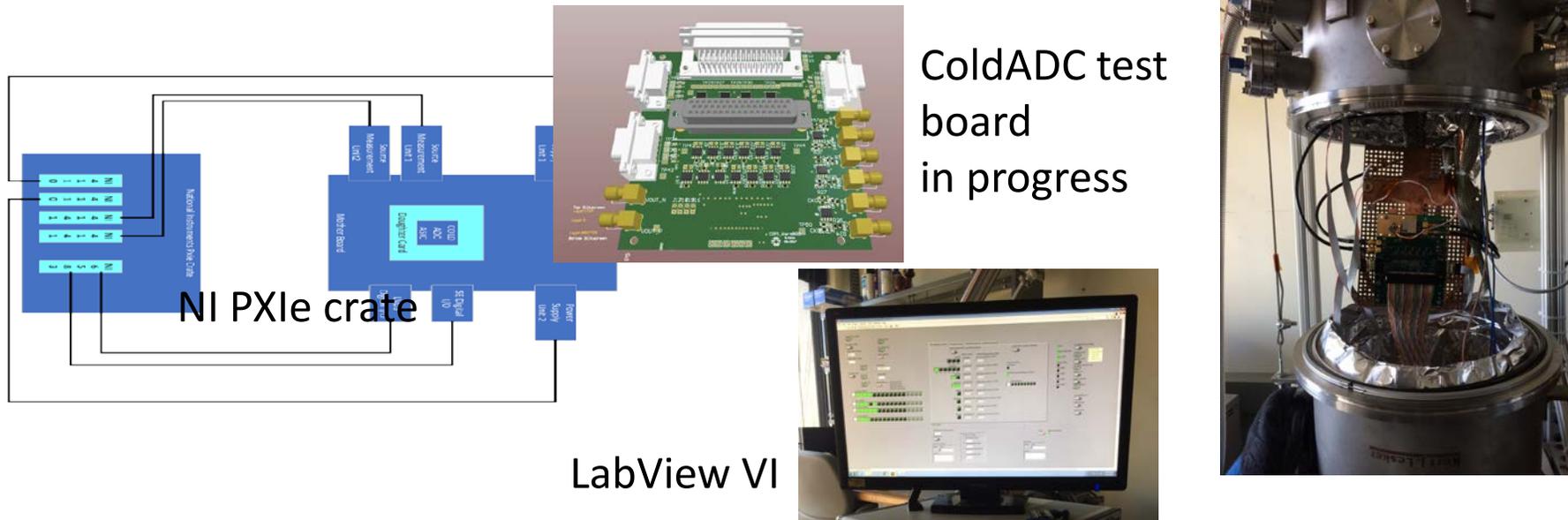
Mu2e Tracker

Vadim R

- Lowest mass tracker ever built in HEP
- 216 modules like above
- Operate in vacuum, high radiation area all electronics on the detector
- 50ps ΔT resolution on two sides (Jin-Yuan's TDC)
- High power inductor-less DC/DC (Dave H.)

Cold Electronics for DUNE

- ColdADC v1 in Fabrication, due 2nd half Jan. 2019
 - Jim, Sandeep, Davide, Alpana, collab. with BNL and LBNL
 - Scott - Test stand in preparation (below)



- Next: COLDATA v1 in design – submission Feb./Mar. 2019
 - Jim, Sandeep, Davide, Alpana collaborating with SMU

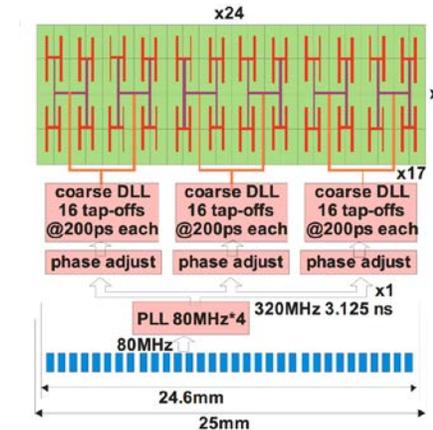
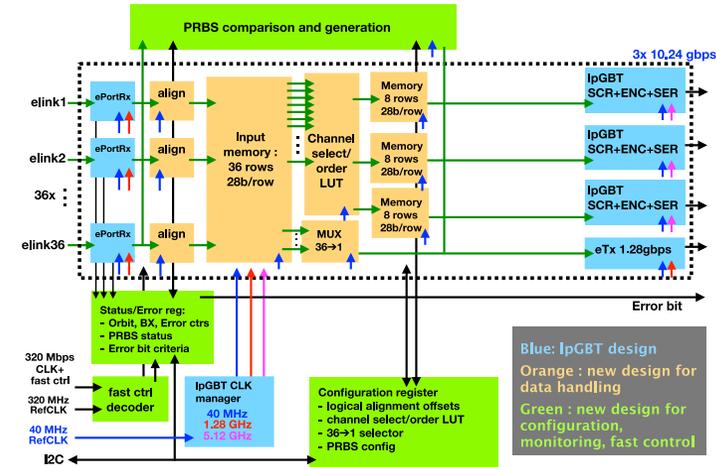
ECON (CMS High Granularity CAL)

- Endcap CONcentrator Prototype 1
 - Aggressive design with Gbps inputs & outputs
 - All I/O functionality
 - Front-end error handling & sync.
 - Clock generation with IpGBT clock manager
- Jim, Gregory, Sandeep with CERN & BNL collaboration

ETROC *a.k.a. FanTastIC* (CMS Endcap Timing Layer)

- Readout of Low Gain Avalanche Detectors (LGAD)
- with 50 ps timing resolution
- Fermilab and SMU collaboration
 - ASIC Engineer Quan Sun joined Fermilab from SMU, continues ETROC design with Tom, Farah will do custom PLL
 - Electronics and FW – Jamieson

ECON p1 concept



NECQST: Novel Electronics for Cryogenic Quantum Sensors Technology

- Recently awarded \$430K funding for QuantISED (HEP Quantum Information Science Enabled Discovery)
- Two-year collaboration between **Fermilab, GeorgiaTech, JPL and Caltech** for developing low-noise cryogenic readout circuits for **superconducting nanowire single photon detectors (SNSPDs)** based on state-of-the-art, commercially available **SiGe HBT** technology, operating at a range of **1-4 Kelvin**.
- Led by Fermilab (**PI Davide Braga**), which will focus on the modelling and characterization of transistors, with the creation of custom, EDA-ready libraries, to be used in the development of cryogenic amplifiers specifically designed for SNSPDs.
- Fits into broader initiative for developing cryogenic testing and modelling capabilities at Fermilab, with the addition of a 4K dry testbed and software tools, which can benefit also cryogenic detectors (LAr) and dark matter searches

New 4K cryostat



RD53SEU Test Chip

- Sandeep, Lou, Pam

- Objective

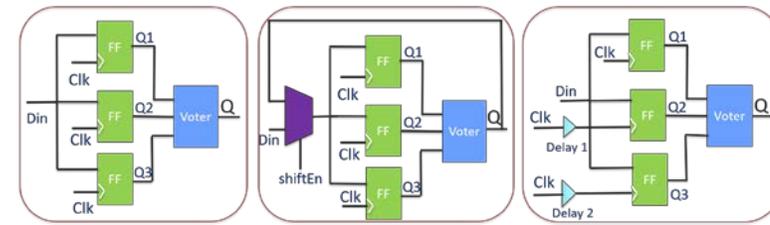
- Study the Single Event Effects on a Triple Modular Redundancy (TMR) logic
- Measure Single Event Transient (SET) glitch width
- Study SEEs on a DICE latch, POR, E-Fuse

- Project collaborators

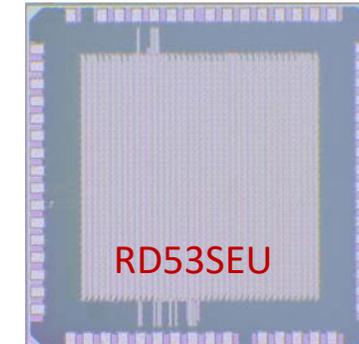
- Fermilab, CPPM Marseille, Univ. of Sevilla & Univ. of Bonn
- Realized under the frame work of RD53

- Chip design and status

- 65nm process, 2mm x 2mm, Submitted in Aug 2018
- Chips are wire bonded to daughter boards
- Firmware is in progress, functionality testing in a week
- Plan is to carry out ion beam testing at two facilities (Europe and U.S)

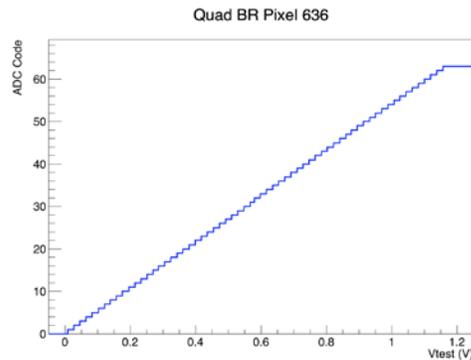
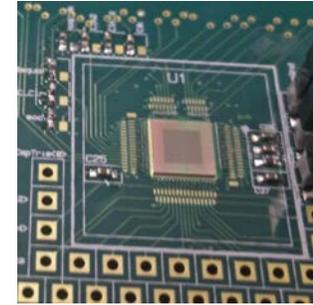


TMR versions investigated

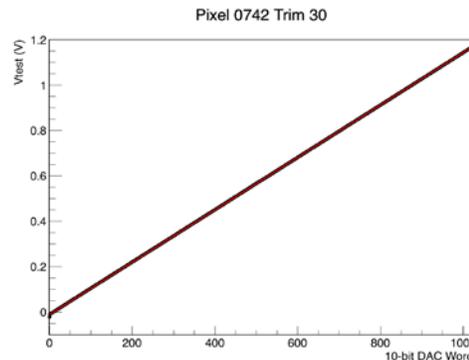
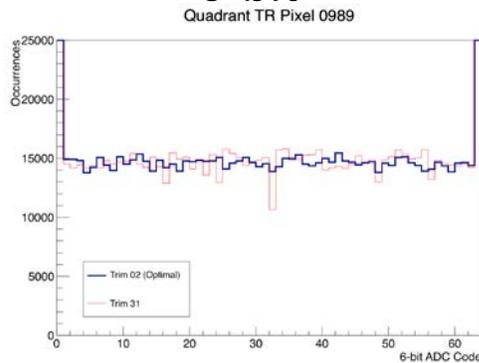


FLORA (Fermilab-LCLS CMOS 3D-integRated detector with Autogain)

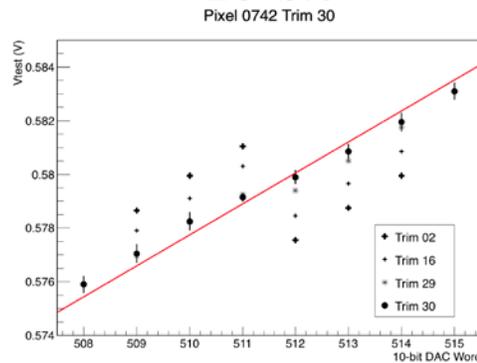
- Farah, Tom, Gregory collaboration with BNL (was SLAC)
- Testing finished, data analyzed –Tom, Lukasz (Krakow), Pam
 - Entire chip tested at 6 bits and 10-bit measurements made
 - Only 2% of 4096 pixels bad
 - FLORA NEXT proposal in preparation, paper and report imminent



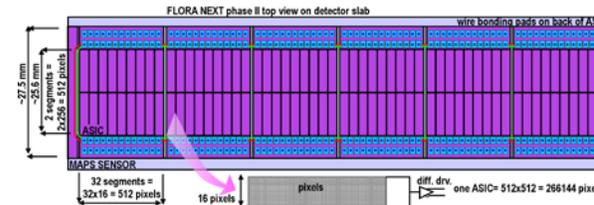
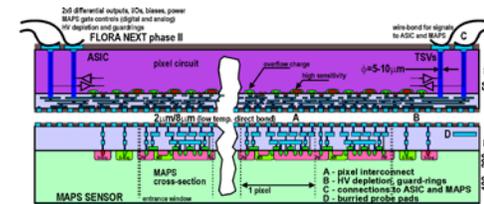
6-bit



10-bit



FLORA NEXT Phase II concept Large Scale HDI Sensor-to-ASIC



(see next slide)

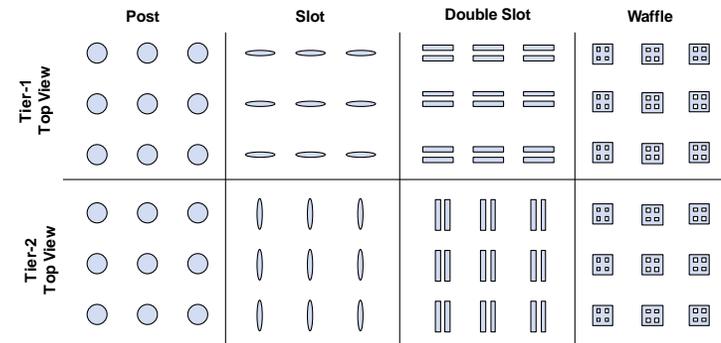
High-Density Interconnects (3D Integration)

- G. Deptuch collaborating with BNL and MIT-LL
- SOW written & working with procurement (Pam) to advance
- MIT-LL has licensed Ziptronix process
- Two phase effort to demonstrate DBI[®] process
 - Phase 1 – Fermilab funded
 - DBI layers in four configurations
 - Pitch as small as 10 μm
 - Posts as small as 1 μm
 - After bonding, perform electrical tests to measure yields
 - Phase 2 – Brookhaven funded
 - Select DBI geometry with highest yield
 - Modify masks and top metal layers
 - Perform electrical tests to establish yield



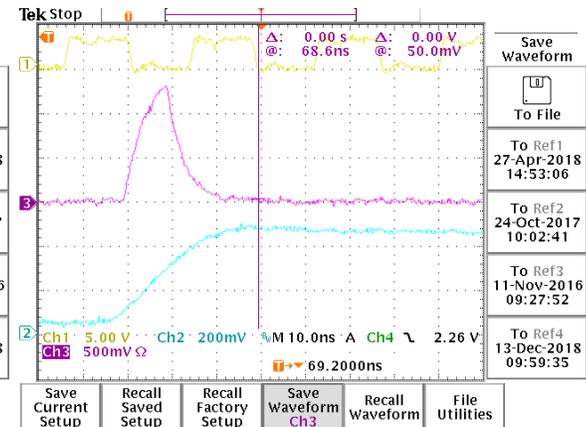
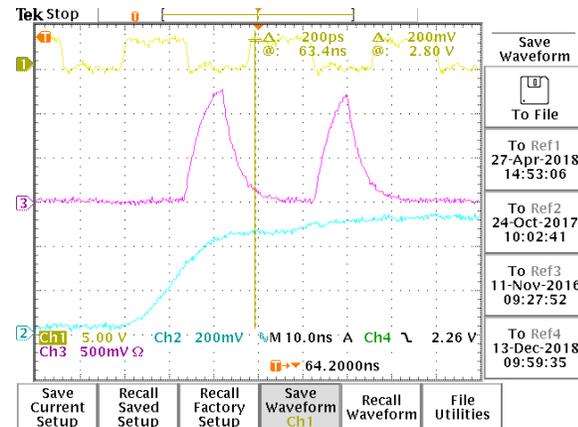
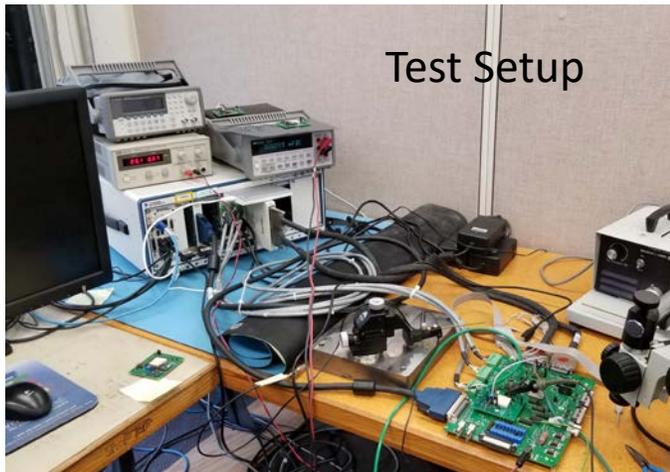
LINCOLN LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
244 Wood Street, Lexington, Massachusetts 02420-9108

STATEMENT OF WORK
for
Development of High-Density Wafer-
to-Wafer Interconnects to Enable
Next-Generation Scientific
Instruments for HEP and BES



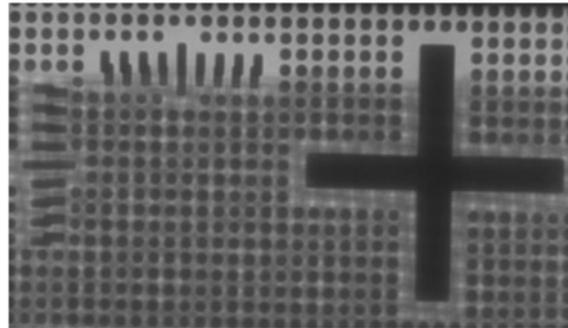
FCP130v2 ASIC

- Overall Characterization and functionality testing of the FCP130v2 ASIC performance – Lou, Farah, Tom
 - Beam studies with Bump Bonded sensors of different type.
 - Intense studies of pixel hit and ADC flash data comparators.
 - Studied ASIC tolerance to leakage currents at input.
 - Studies of a new Conflux Data Transfer Technology design (Functionality, Speed and Reliability tests).
 - Studies of sequential pixel hits (lower left).

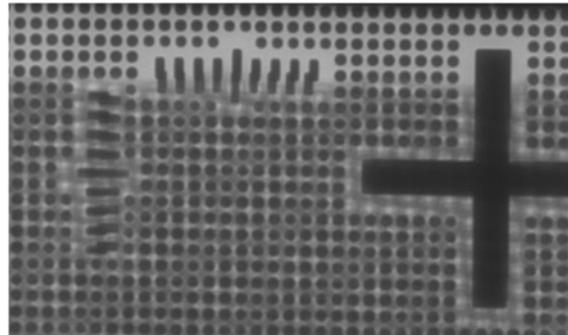


VIPIC-L and VIPRAM

Internal FNAL 3D-IC run - GF130 nm CMOS process and Tezzaron(Nhanced) / Novati(Skorpios) 3D IC technology with B-TSV Via (VIPIC-L and VIPRAM)

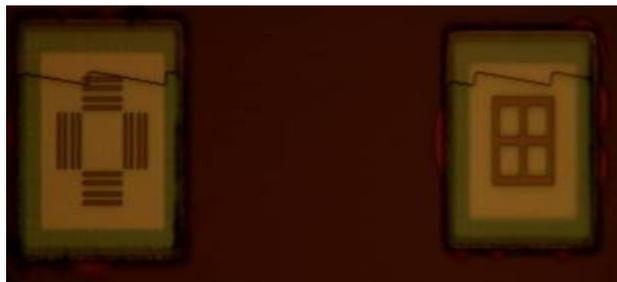


LEFT

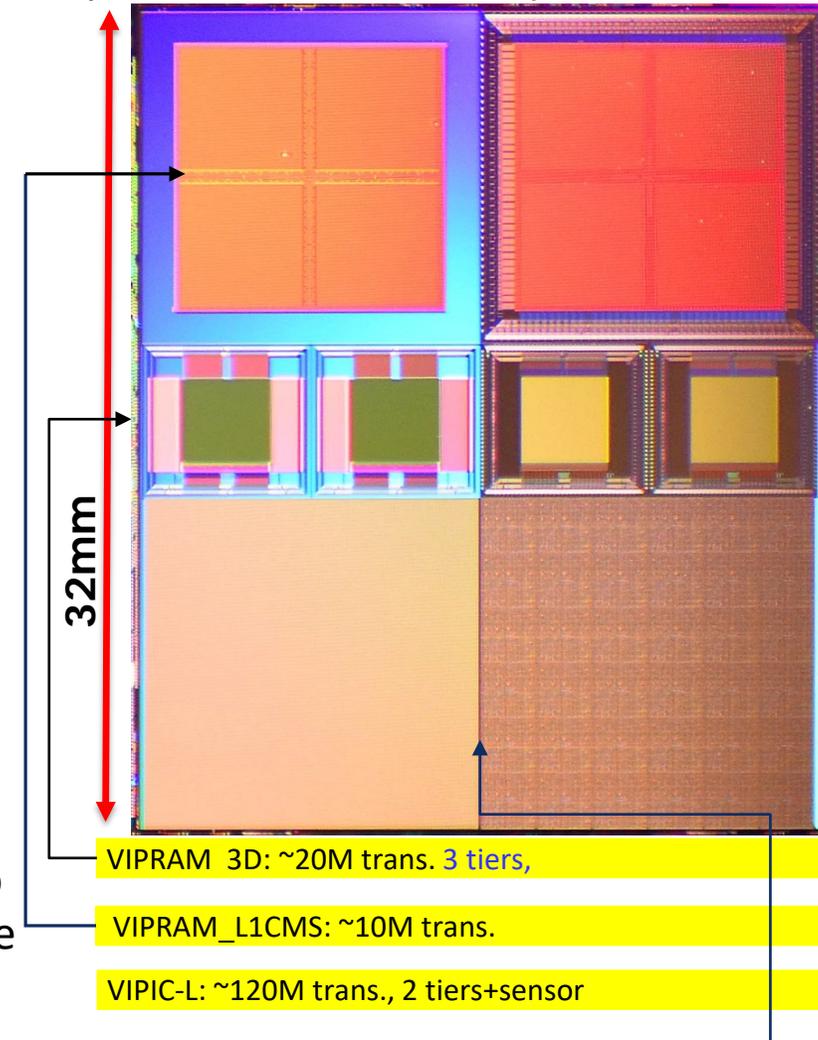


RIGHT

2.5 μ m bonding 'dots' on 5 μ m pitch



opened TSV alignment keys, after digital wafer thinning to 10mm and before B-TSV module



Cleanroom Refurbished

AI - The cleanroom had not been touched since ~1995!

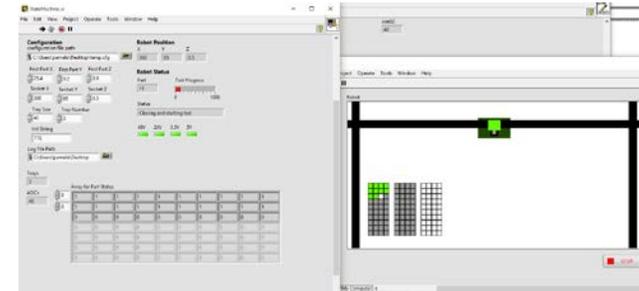


Plasma cleaner in action! (movie)

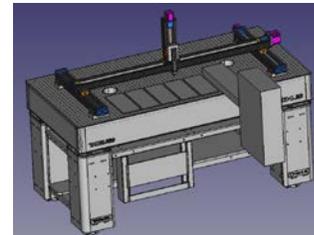


More Projects

- **FASPAX** – Tom, Farah, Gregory, Davide
 - Testing completed, paper for ULITIMA proceedings (NIM A)
- **VIPRAM** – Procuring a bump-bonded version to test - Pam
- **VIPIC-L** – testing in 2019 – Scott
- **Polsky & Energy iCorps** (commercialization) – Farah
- **Four US Patents**
 - 9,923,017 9,928,202 10,075,657 10,084,983
- **New Robot** – Pam
 - Core robot components selected
 - Software development in interim
 - State machine, User GUI
 - Animation
 - Log and config files



GUIs



Robot MCAD

Good bye 2018

- Busy but excellent year
- We are doing many projects, across the lab and across the world
- Things are getting done!!
- We have a dynamic department and new people coming in
- Looking forward to 2019 as per Forbes:
 - “best friend” medal
 - World at the lowest level of happiness since 2006 according to Gallup (Alexa, bring me joy)
 - Exoskeleton boom (robotic underwear)
- Enjoy the well deserved holiday break!



Thank you Everyone!

