Fermilab

Managed by Fermi Research Alliance, LLC for the U.S. Department of Energy Office of Science

PCB design with Altium

Vadim Rusu

EED group meeting

12/13/17

Altium @EED

- Over the last year we transitioned from Mentor tools to Altium
  - many people on the floor were using Altium before
  - goal was to come up with a comprehensive tool to support PCB design in the future
  - learning the tool, while not easy, it is straightforward
  - hard part is developing and integrating all supporting infrastructure
  - many people involved: Nina, Rod, Jamieson, Paul, and others

Altium Intro

- We (thanks Jamieson) are trying to keep a “help” web page with useful info, tutorials, etc.
  - http://altium.fnal.gov

Altium Home Getting Started Vaults Guidelines Help Fermilab

1. Getting Started

1.1 First Time Setup

1. Create an AltiumLive account here
2. Download and install the latest version of Altium
3. Request a Fermilab Vault account from Jamieson or Vadim
4. Launch Altium and Setup Private License Server (DXP ⇒ My Account ⇒ Admin ⇒ Setup Private License Server):
Private License Server = altium.fnal.gov:21001

5. Add the Altium Content Vault and Fermilab Vault (in DXP ⇒ Preferences ⇒ Data Management ⇒ Vaults)

Preferences

Cloud Preferences

System
Data Management
Version Control
Design Repositories
Vaults
Publishing Destinations
Backup
File Locking

Data Management – Vaults

Vaults

A vault stores structured and revisioned data that is characterized by lifecycle states.

Name	Description	Address	Status	Enabled
Fermilab EED Vault	Fermilab EED Vault	http://altium.fnal.gov:9780/vault/		

Altium Vault

- Storage, component management, workflow management, concurrent version support
- To the end user, they are really trying to make it like a simple directory structure
  - There is a Sandbox directory, abuse it.
  - Nothing gets deleted from the Vault, instead items get moved to Trash
  - Most people will only care about Components and the Search field
- Altium provides Altium Vault, lots of components there
  - We should use an item if it's already there

Altium Vault

- As of now, there are 34 registered EED Vault users
  - people from other divisions too
  - there are built in mechanisms to give priority to the department

Administrators	4
Engineers	23
Librarians	4
Managers	1
Visitors	8

Project management

- really, version control and concurrency
- I can speak here from my own experience, did 5 PCBs with Dave H. and worked great - a lot better than sending design screenshots back and forth
- there are about 30 projects now in the vault

Name	Author	Last modified	Open	Edit	Share	Remove
MPPC_Main_board Managed project "MPPC_Main_board" created from AD	nmoibenk	12/11/2017				
ColdADC2017b1 Cold ADC board Jin-Yuan Wu	nmoibenk	12/11/2017				
MPPC_holder_board Managed project "MPPC_holder_board" created from AD	nmoibenk	12/11/2017				
LidBoard2 Lid Board by Mike Utes	jtoadmin	12/8/2017				
RPS Rack Protection System	huffman	12/6/2017				
CapLoad208V20A Managed project "CapLoad208V20A" created from AD	huffman	12/5/2017				
MPA-Probe-Card Managed project "MPA-Probe-Card" created from AD	los	12/5/2017				

Part libraries

- OK, no such concept in the vault, but part directories
- Nina did a lot of work uploading people's libraries in the vault
  - PLEASE USE THEM INSTEAD OF LOCAL COPIES
- PLEASE REQUESTS PARTS

ID							All
PR-43	17.09.06 13:26	4-Bit Bus Transceiver with Configurable Voltage Translation and 3-State Outputs in 16-pin TSSOP p...	Texas Instruments	SN74AVC4T245PW	holm		Completed
PR-42	17.08.29 09:21	COLD Data ASIC	Fermilab - EED - ASIC	CDP1	holm		Completed
PR-37	17.08.28 09:03	40 MHz oscillator	SiTime	SiT5001AI-GE-18NO-40.000000	holm		Completed
PR-36	17.08.22 13:50	VHDCI 0.8mm R/A Receptacle	ALL Best	R-HS-008068-1B	holm		Completed
PR-35	17.08.22 13:15	Low Voltage 1.2v/1.8v CML 1:2 Fanout Buffer, 3.2GBPS	MICREL	SY54011RMG	holm		Completed
PR-34	17.07.17 15:01	CONN HEADER 50POS .8MM DUAL SMD	SAMTEC	FTE-125-01-G-DV	holm		Completed

Altium@EED Overview

- Altium updates relatively often, I'd recommend keeping up with the updates
- At this point, we have 6 Altium licenses (+2 SE)
  - however, FNAL has a total of 12
    - something we need to further look into
- There are 12 Altium Vault CAL licenses.
  - What this means is that 12 people can be simultaneously using the Vault.
  - There is a 12 hours timeout
- EED Altium Vault is backed up weekly Saturday at 4AM (thanks Rod)
  - we should soon start deleting old backups (~2GB/backup)

Projects

- Projects start from a Configuration
  - Design Rules, templates, BOM-Active and Standard Output Jobs
  - Only one now in (EED Design)
    - I don't think this is used properly
    - Unfortunately it may take some time to mature
  - Once done, entire project should be archived to Vault (including output jobs, documents, etc.)
    - To my knowledge we have not done this yet

Wrapping up…

- I think at this point we have a set of comprehensive tools for PCB design and part management
- Still to do:
  - More part requests
  - Start taking care of the component lifecycle
  - Template designs?
  - Periodic vault cleanup?
  - Anything else?

Some more stuff on components

Altium Components

- A component is a collection of models, specifications and supply chain information
  - Models:
    - schematic symbol (SchLib)
    - footprint (PcbLib)
    - simulation (yes, SPICE is integrated in)
    - signal integrity
  - Specifications:
    - datasheet,, description and whatever else one can think of
    - keywords should be in description, helps to search
  - Supply Chain
    - real time stock, price, vendor part number
    - We should really try to have this in for all components in the EED Vault.
  - Note: The Vault enforces none of this, so group policies have to

Components (cont)

- Search for the component you want in EED Vault.
  - search field can be anything related to that particular comp.
    - Lots of things might pop up, so careful choosing
- If not found, search the Altium Vault
- Finally, Part Request. Here is how it works
  - Part Request goes to Librarian (Nina, with me and Jamieson as backup for now)
    - Specify as much as you can in that part request: Mfg. PN and data sheet should be minimum
    - Once the part request is completed you will receive an email confirming that the component is now ready to use.
      - Nobody is infallible, so checks are always welcome.
- Components have “lifetimes”
  - Right now, all our comps are “New From Design”
  - As we work the system, they will get promoted (“Prototype” and “Production”)
  - Once promoted to “Production” ulterior usage rock solid.

Fermilab

PPD / EED / Infrastructure & Support Group

Fermilab

Who are we?

Johnny
Walter
Curtis

Victor
Dave H.
Tim
Steve
Rod
Mike M.
Mike C.

Nina
Paula
Jacob
Dave F.
Arnab
Tyler

Fermilab

Weeee!

Fermilab

What do we do?

Administer / Maintain Networked Design Tools.
Administer / Maintain Wilson Hall Ground Floor PPD Tech. Shop.
Assembly / Design / Repair of AC Power Distribution Systems.
Assembly / Design of Cable Harnesses.
Assembly / Design / Repair of DC Power Distribution Systems.
Assembly / Design / Repair of Equipment Chassis.
Assembly / Design / Repair of Equipment Racks.
Assembly / Design / Repair of Rack Protection Systems.
Assembly / Design / Repair of High Power Distribution Systems.
Assembly / Design / Repair of Printed Circuit Boards including high performance rigid and flexible.
Computer Aided Drafting and Engineering.
Computer Application Development.
Computer System Analysis.
Coordination of Contract Fabrication and Assembly.
Electrical Safety Reviews, including Operational Readiness Clearance.
Engineering Design Reviews.
Fabrication of 3D Printed Structures for prototype and production.
Fine Surface Mount Component Soldering.
Installation / Maintenance of Cable TV Systems.
Installation / Maintenance of Internet Protocol Camera Systems.
Modification of Existing Premise Wiring, including System Design, Cost Estimation, Procurement of Required Supplies / Equipment and Electrician Supervision.
Printed Circuit Board Layout - simple to complex.
Provide Guidelines for Cable Selection.
Provide Guidelines on Electrical Design Standards.
Provide Project Life Span Guidance for all Group Capabilities.

Fermilab

Some of our customers:

LCLS-II

SBFD

Fermilab AD

ICARUS

PPD / DDOD

HL-LHC US CMS

ANNIE

PPD / EED ASIC

MINERvA

µBooNE

PPI

PPD / DO

SeaQuest

µ g−2

protoDUNE

CDMS

SNOLAB

DUNE DEEP UNDERGROUND NEUTRINO EXPERIMENT

Fermilab ESH&Q Security

US CMS

SMS

Mu2e

PIP-II

Fermilab Astrophysics

SHORT-BASELINE NEAR DETECTOR SBND

Lederman Science Center

Fermilab TD

PPD / MED

FTBF

LArIAT

Argonne NATIONAL LABORATORY

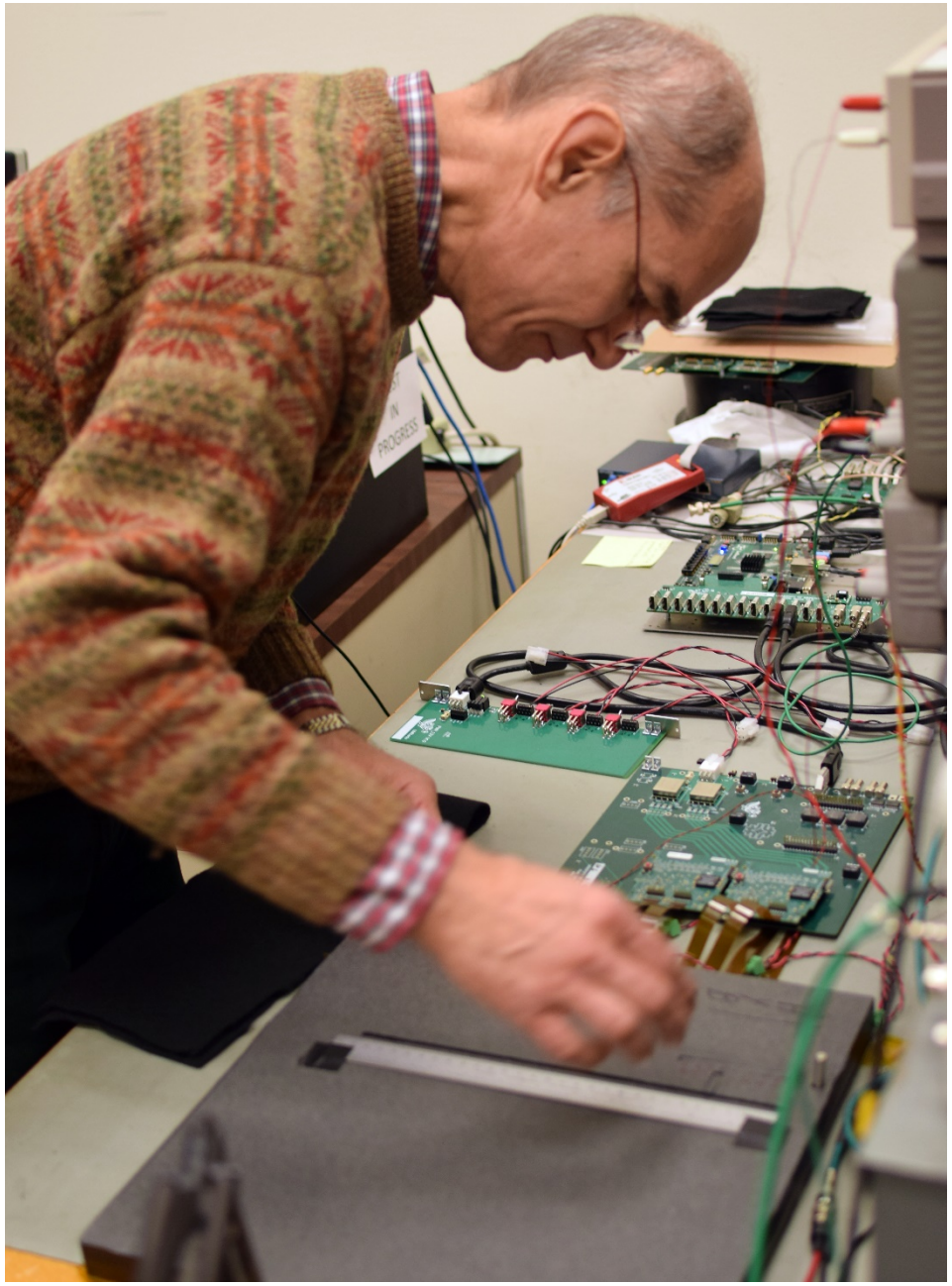
DES / DEC

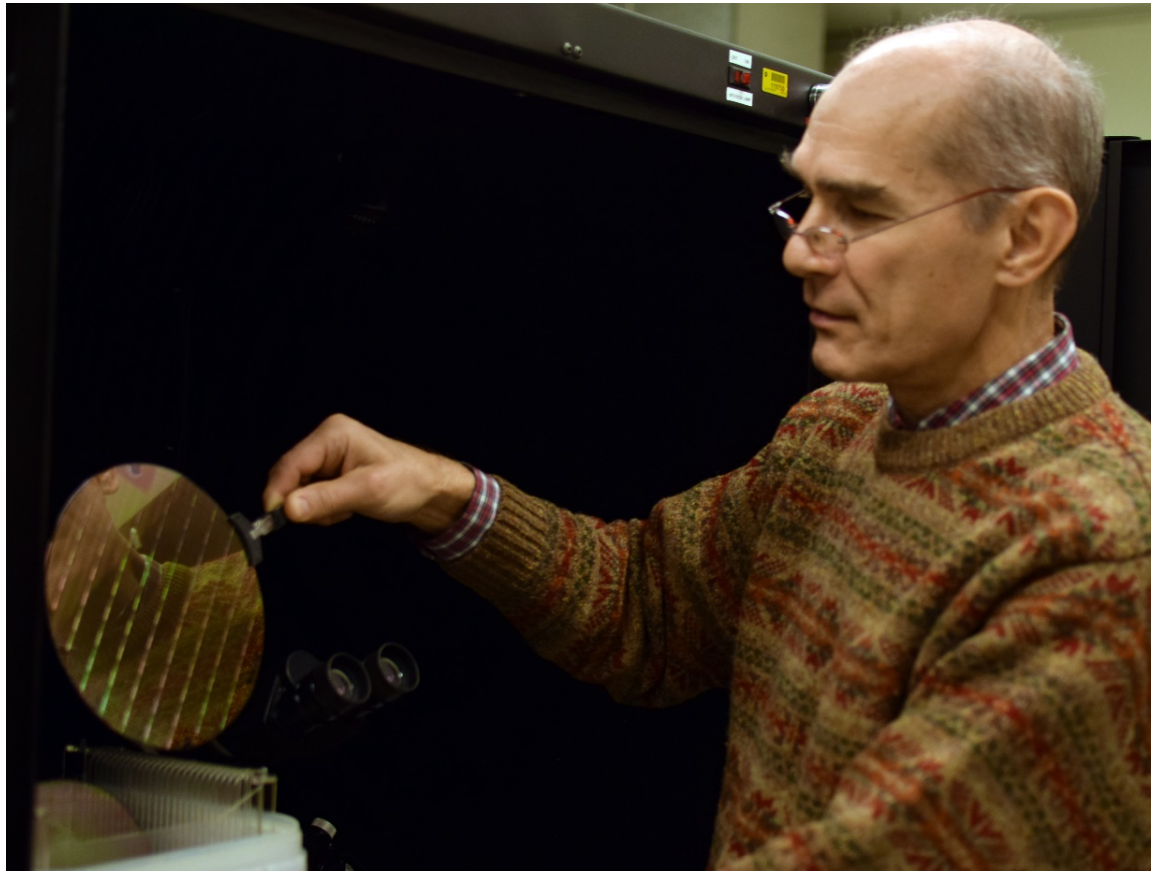
PPD/EED
Detector Electronics Group

13 December 2017

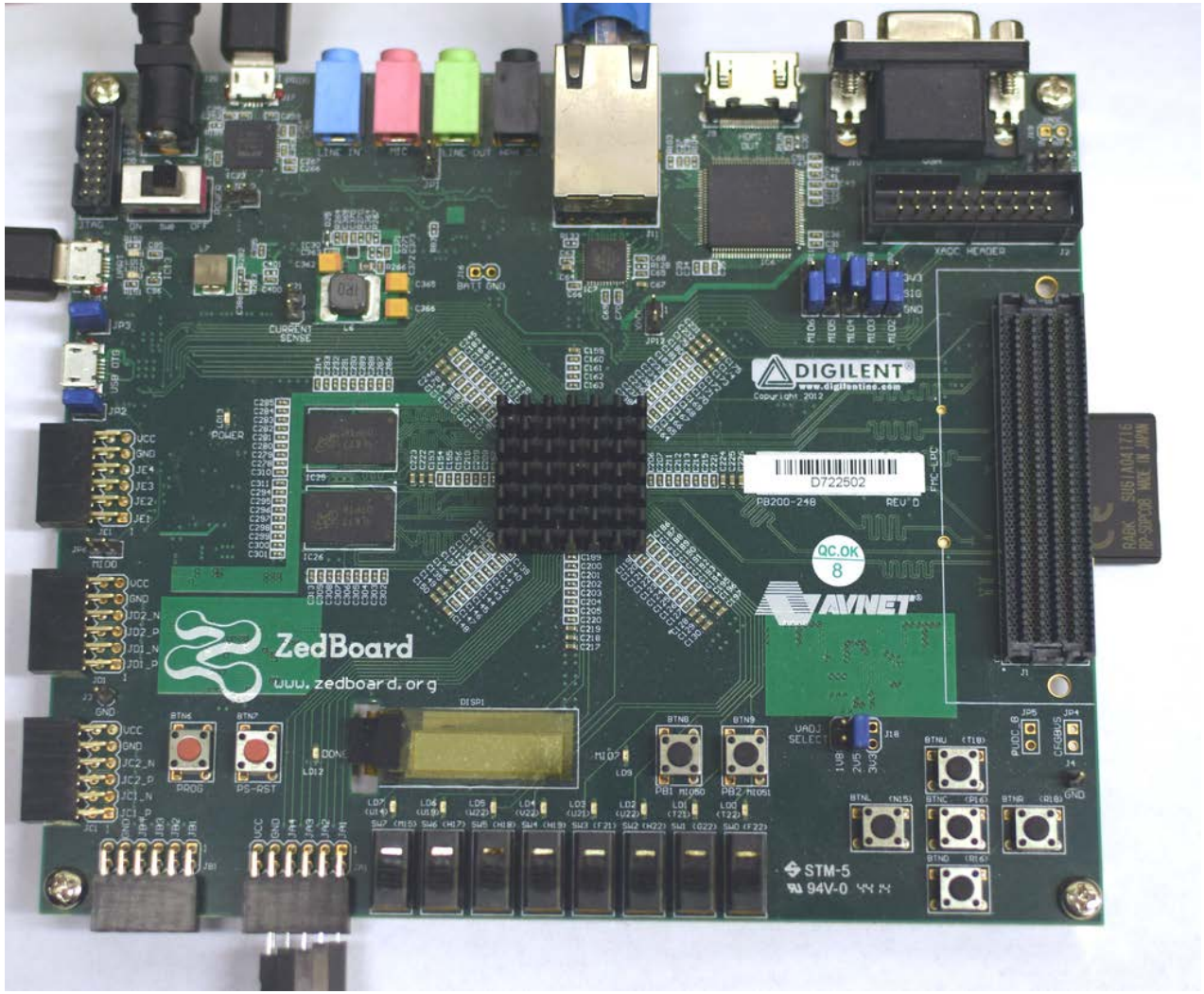
Cristian Gingu

- PHENIX experiment (BNL) Silicon Forward Tracker. FPHX ASIC wafer level testing.
- CMS High Granularity Calorimeter (HGC) firmware on the Xilinx ZYNQ processor. Custom FMCIO board developed.
- CMS HCAL firmware development for boards designed by Terri
- Silicon Muon Scanner firmware and readout software





Wafer level testing for PHENIX experiment. Cristian developed the visual basic software to interface to the test box fixture for automated testing and die marking.

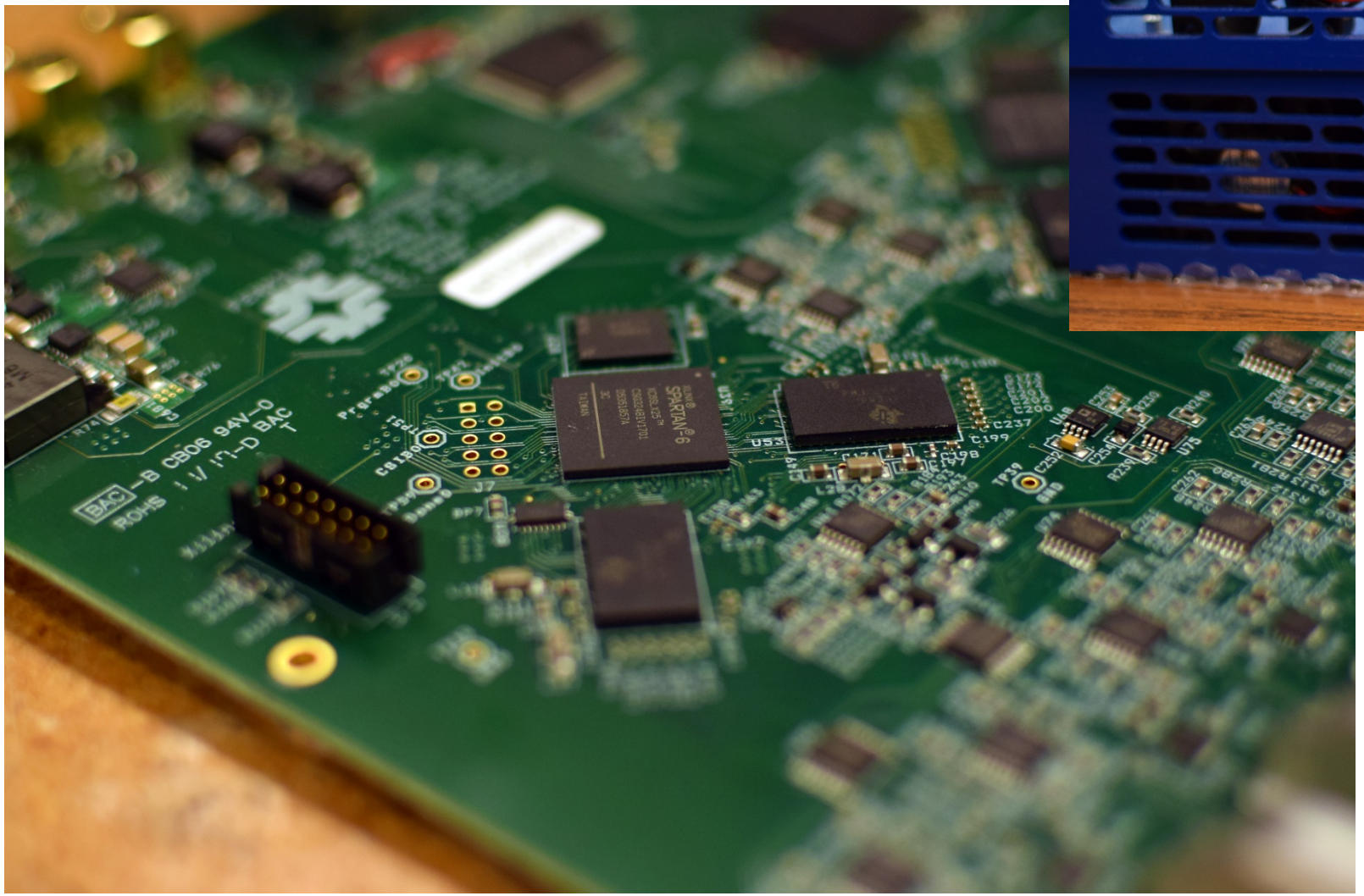


Cristian has been developing {Firmware|Software} For the ZedBoard based on Xilinx ZYNQ processor. This FPGA + multi-core ARM processor can run full Linux OS.

Sten Hansen and Terry Kiper

- Mu2e Cosmic Ray Veto front end boards
  - Pre-production hardware
  - 24 64-channel front end boards
  - Sten = Firmware
  - Terry = Microcontroller code
  - Both = schematics and layout
  - Vertical slice test scheduled for March/April next year.
  - Production of 350 FEBs over next 1.5 years
- CDMS warm electronics. Looking at new revision of our readout card after our Mu2e tests have finished
- MTEST readout controller electronics

Mu2e CRV (Cosmic Ray Veto) front end board detail. Spartan-6 FPGA surrounded by high performance ADC and DRAM chips

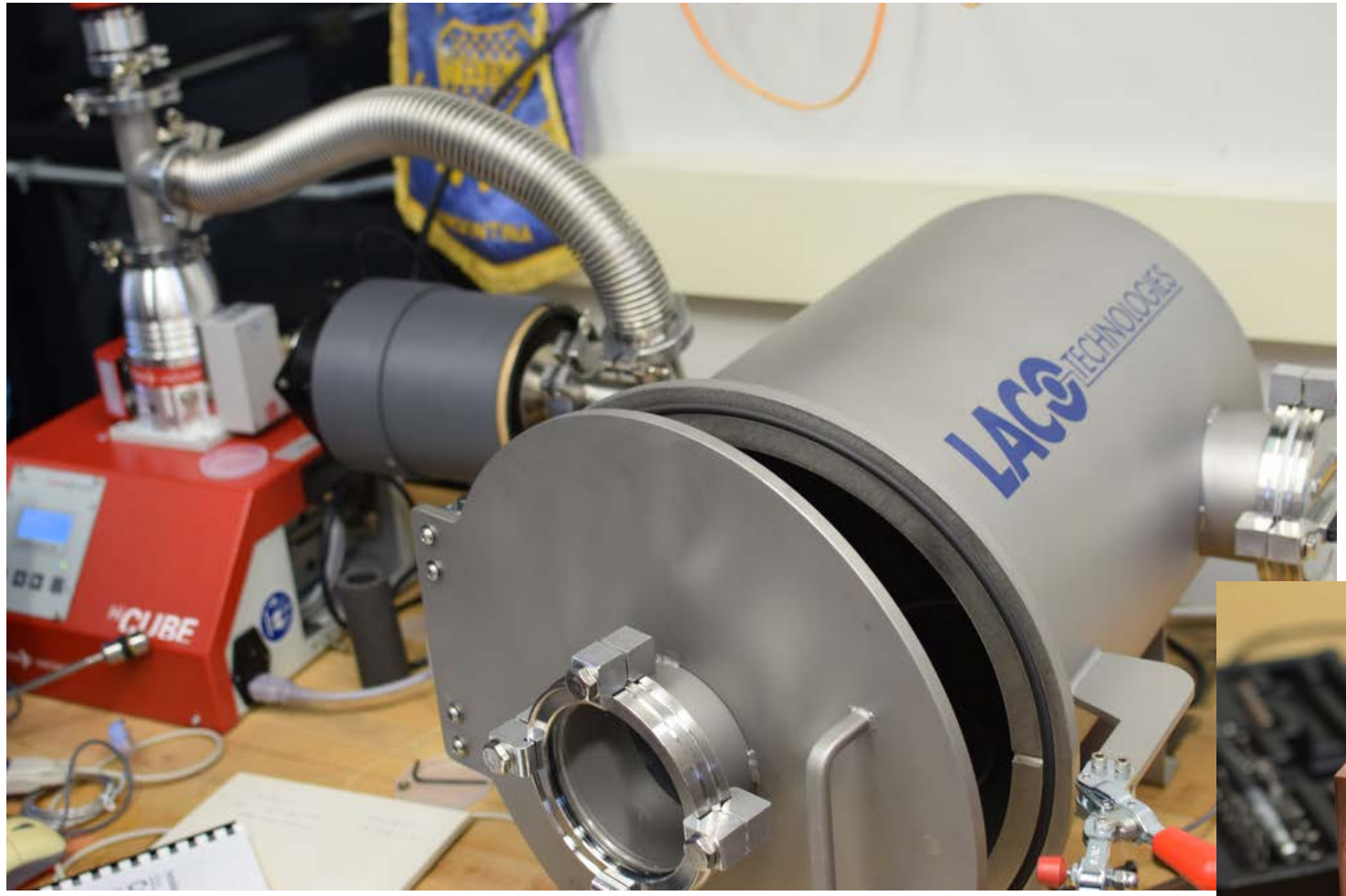


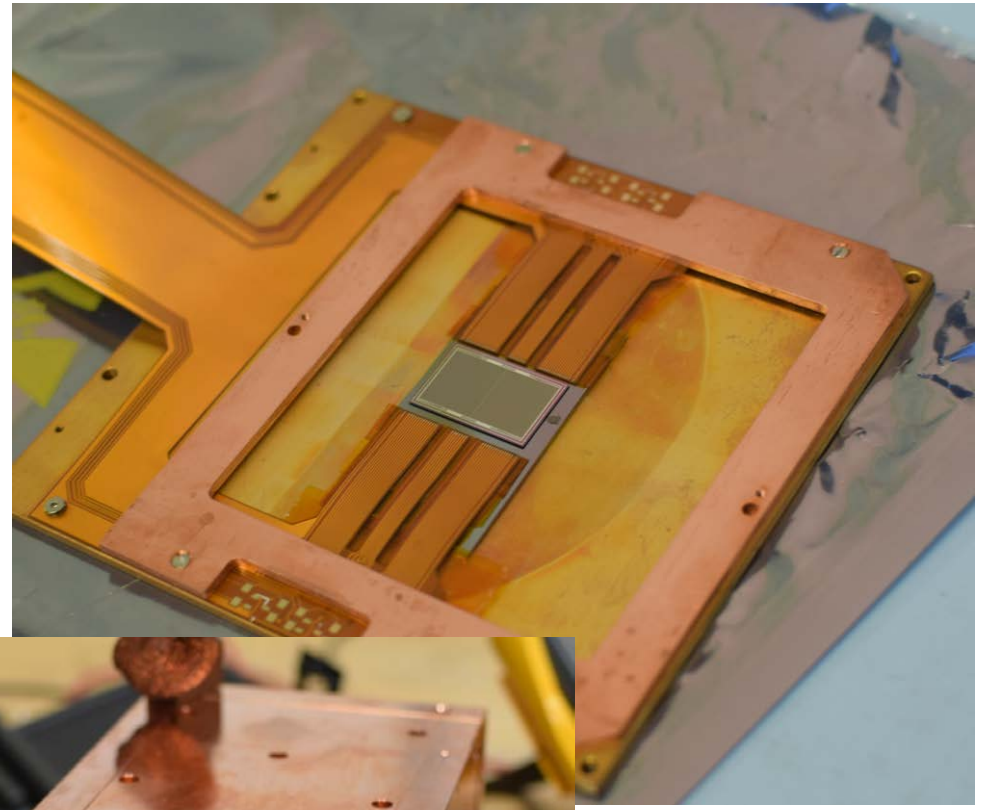
Custom rack mount enclosures designed by Dave Huffman while learning to use NX CAD tools.

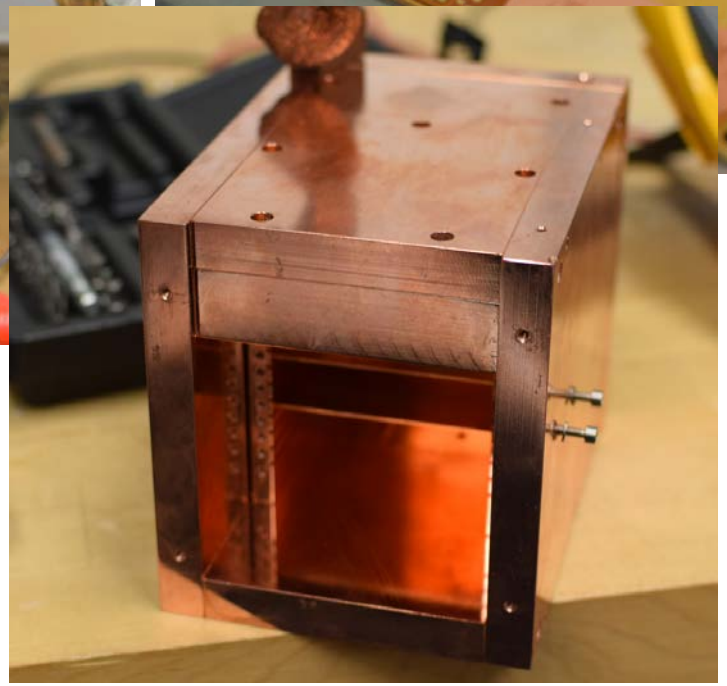
Kevin Kuk

- Building, testing, characterizing CCDs for the DESI instrument.
  - DAMIC, CONNIE, SENSEI
- Microwave Kinetic Inductance Detectors (MKIDs) readout and characterization
- Building a new multiCCD test chamber using a SunPower cryocooler for Skipper CCD production.
- Support of detector installation and fabrication at the SBN-ND.

Kevin with the ADR Cryo (Adiabatic Demagnetization Refrigerator) test stand in one of the SiDet clean rooms.





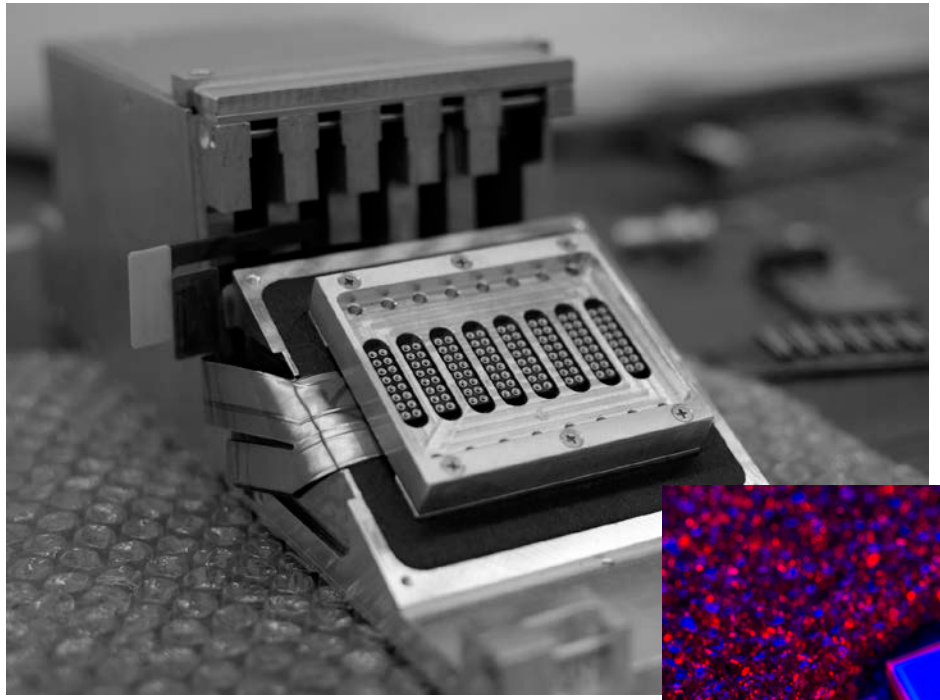


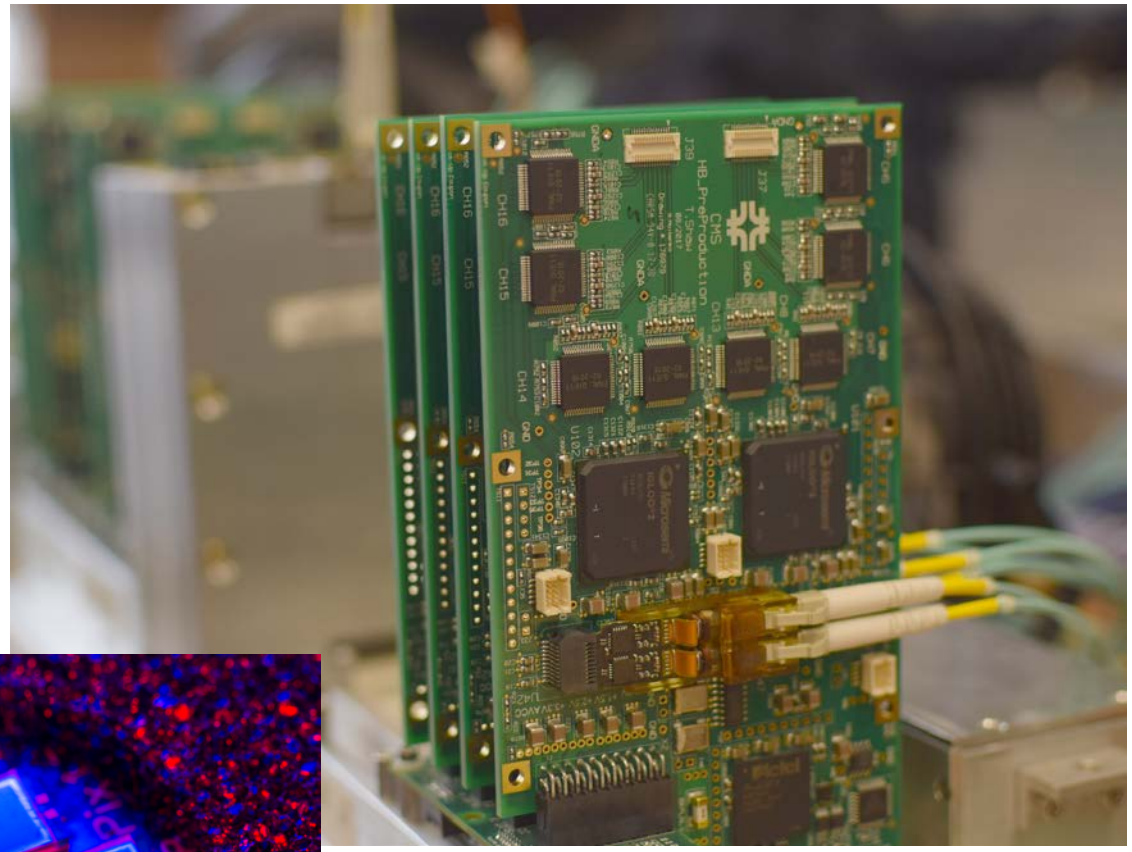
SENSI Experiment “Skipper” CCD packaging and multi-CCD vacuum vessel. Self-contained cryo unit mounts on the side.

Sergey Los

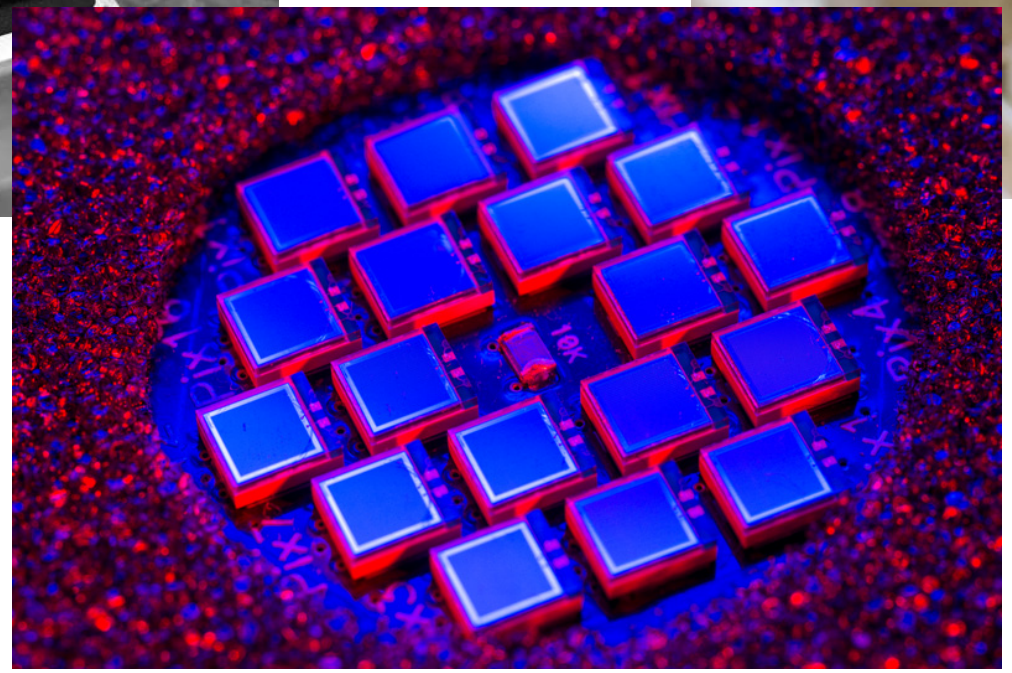
- CMS HCAL Phase 1 upgrade
  - Design of SiPM mounting and control electronics
- CMS phase 2 upgrade HGC (high granularity calorimeter / universal calorimeter) and OT (outer tracker) R&D work
  - probe cards and various test boards
- Precision timing includes boards for LGAD sensors and SiPMs
  - Particle ID and ToF (time of flight)
  - Hardware in use at Fermilab Test Beam Facility (FTBF)
  - R&D now, possible use at CMS…

Mounting board with sockets for SiPM packages. Rear enclosure contains front end cards with QIE ASICs.





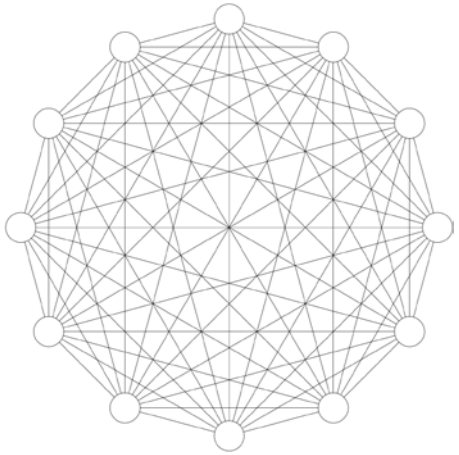
CMS HB-Preproduction board designed by Terri and layout by Nina

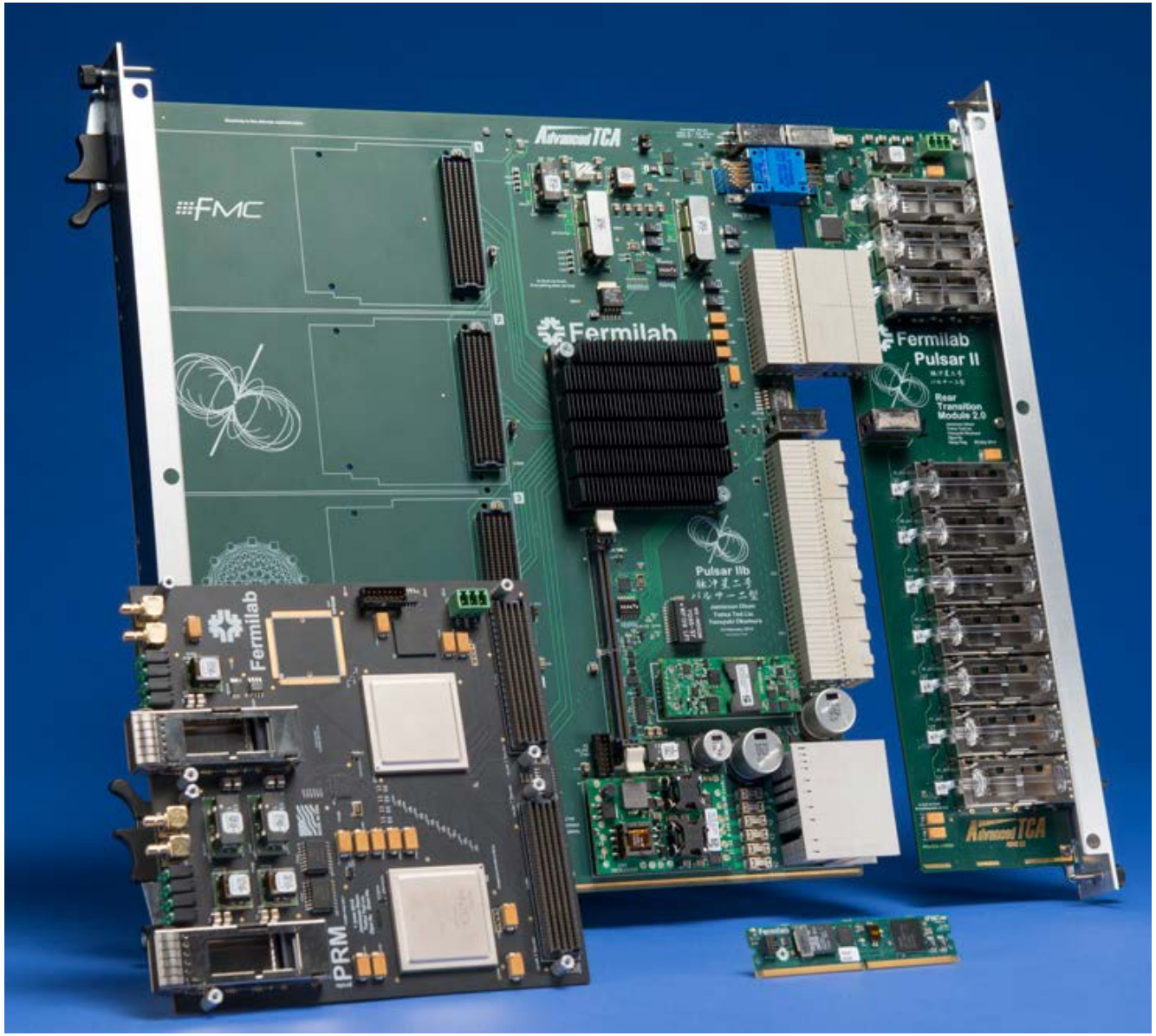


Front-end card with photo-detectors for the CMS Hadronic Outer CAL (HO/HCAL) with control electronics and thermal management.

Jamieson Olsen

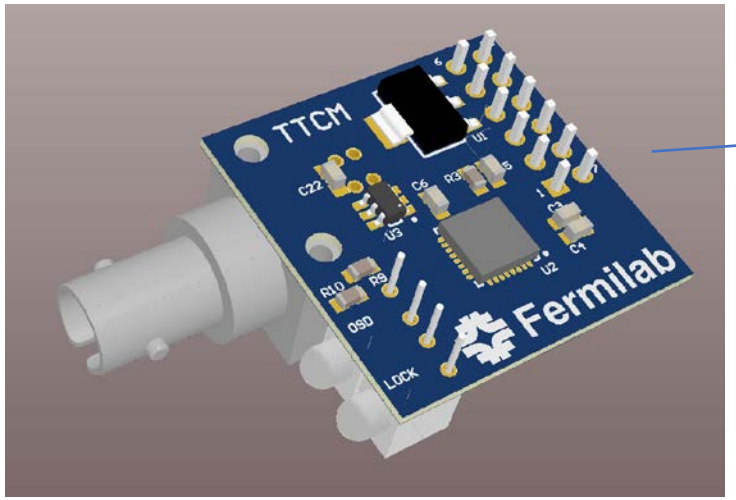
- Working with Ted Liu on Pulsar boards
- Pattern Recognition and Track Finding
- Big FPGAs + ATCA Full Mesh Backplane
- Serial links working at 10Gbps → 25Gbps
- Applications:
  - ATLAS Fast Tracker
  - CMS L1 Silicon Track Trigger R&D
  - Muon Trigger? PET imaging?
- VIPRAM AM ASIC testing
- Interim Group Leader in FY2018
- Supervising two Co-Op students
- Co-Chair, Engineering Promotion Committee





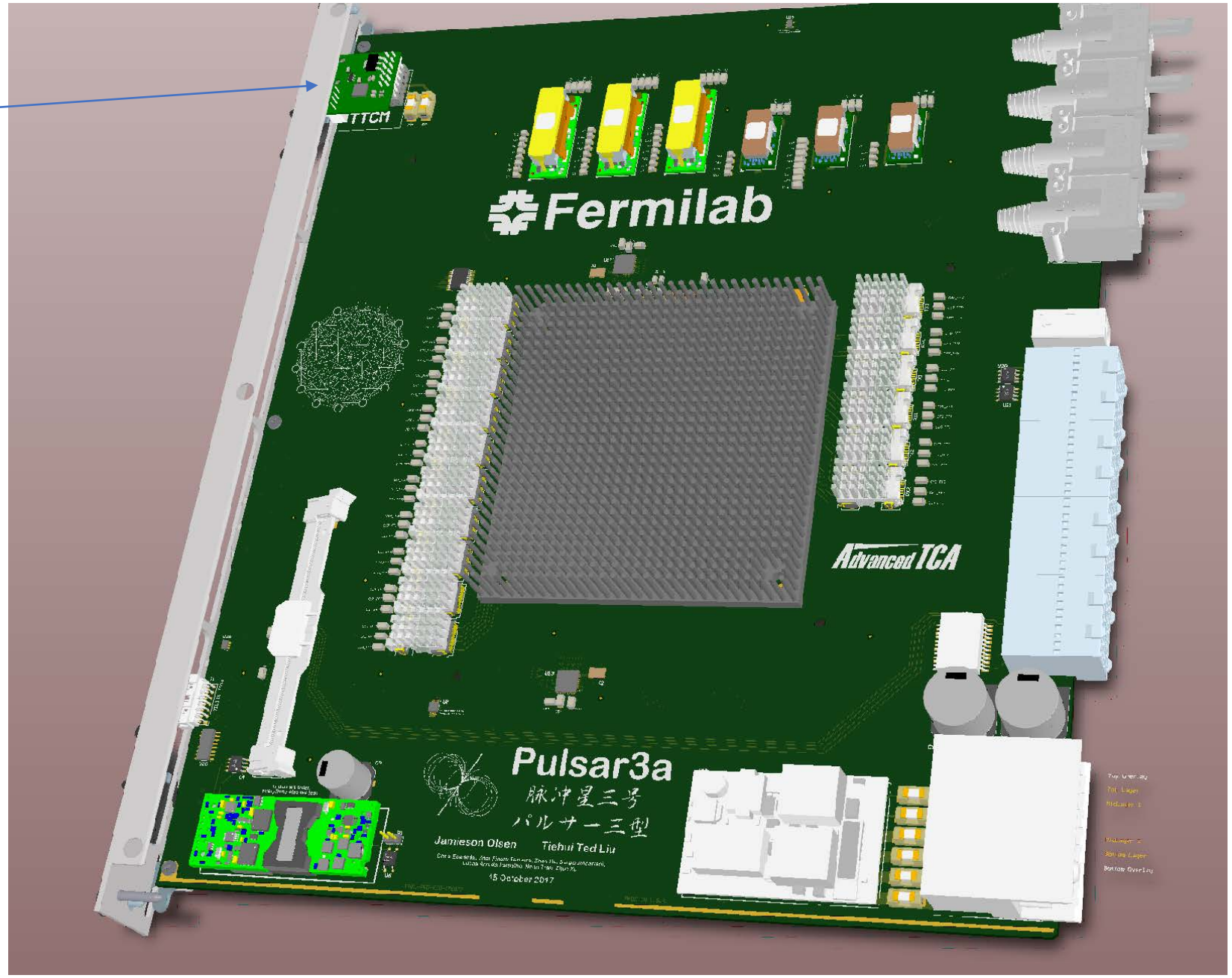
Pulsar2b front board, RTM, and various mezzanine cards

Two ATCA shelves filled with Pulsar2b boards and cabled up with 120 QSFP+ cables = 4.8Tbps



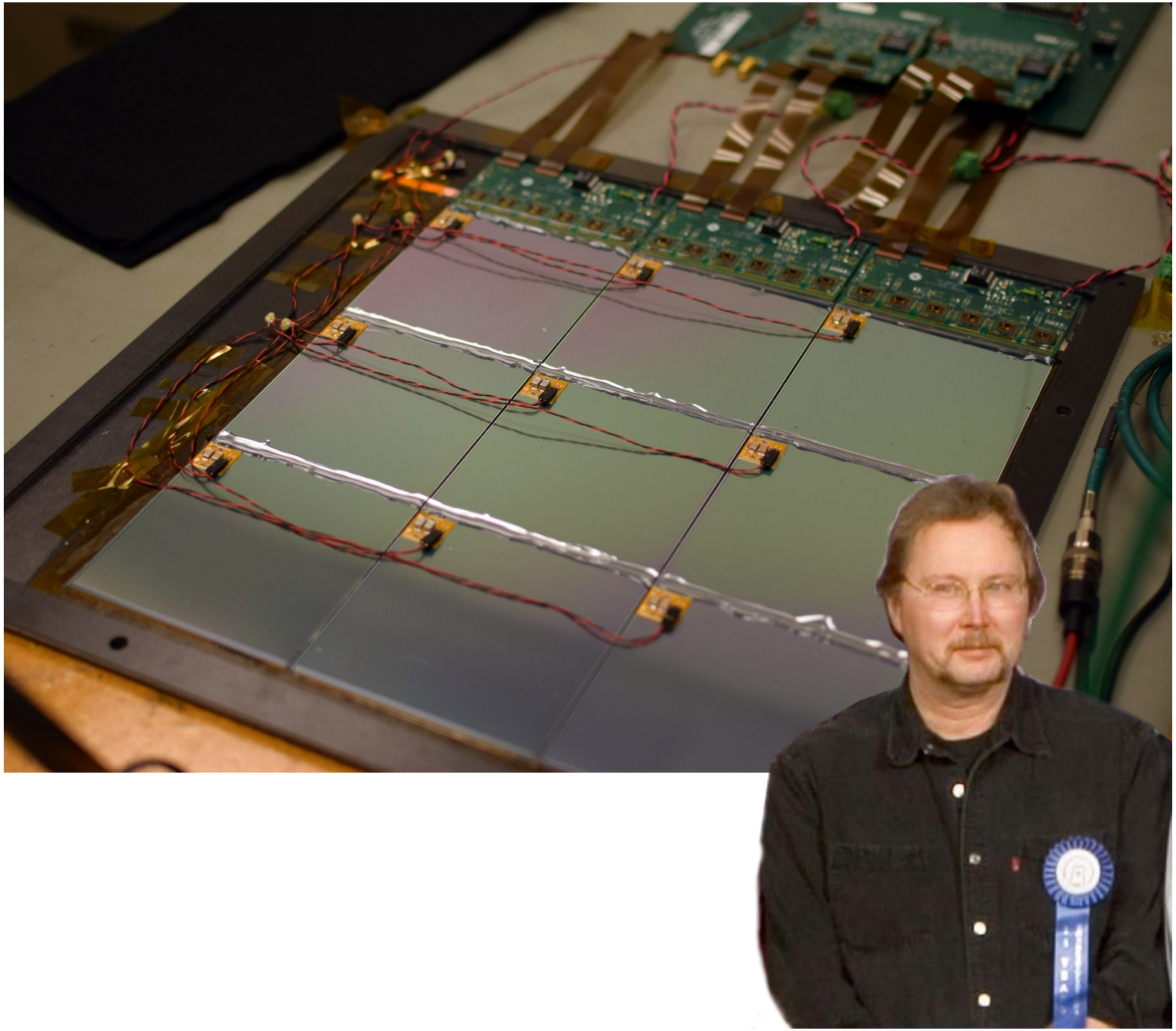
Above: CERN optical Trigger Timer Control (TTC) receiver designed last summer by Co-Op student Chris Edwards.

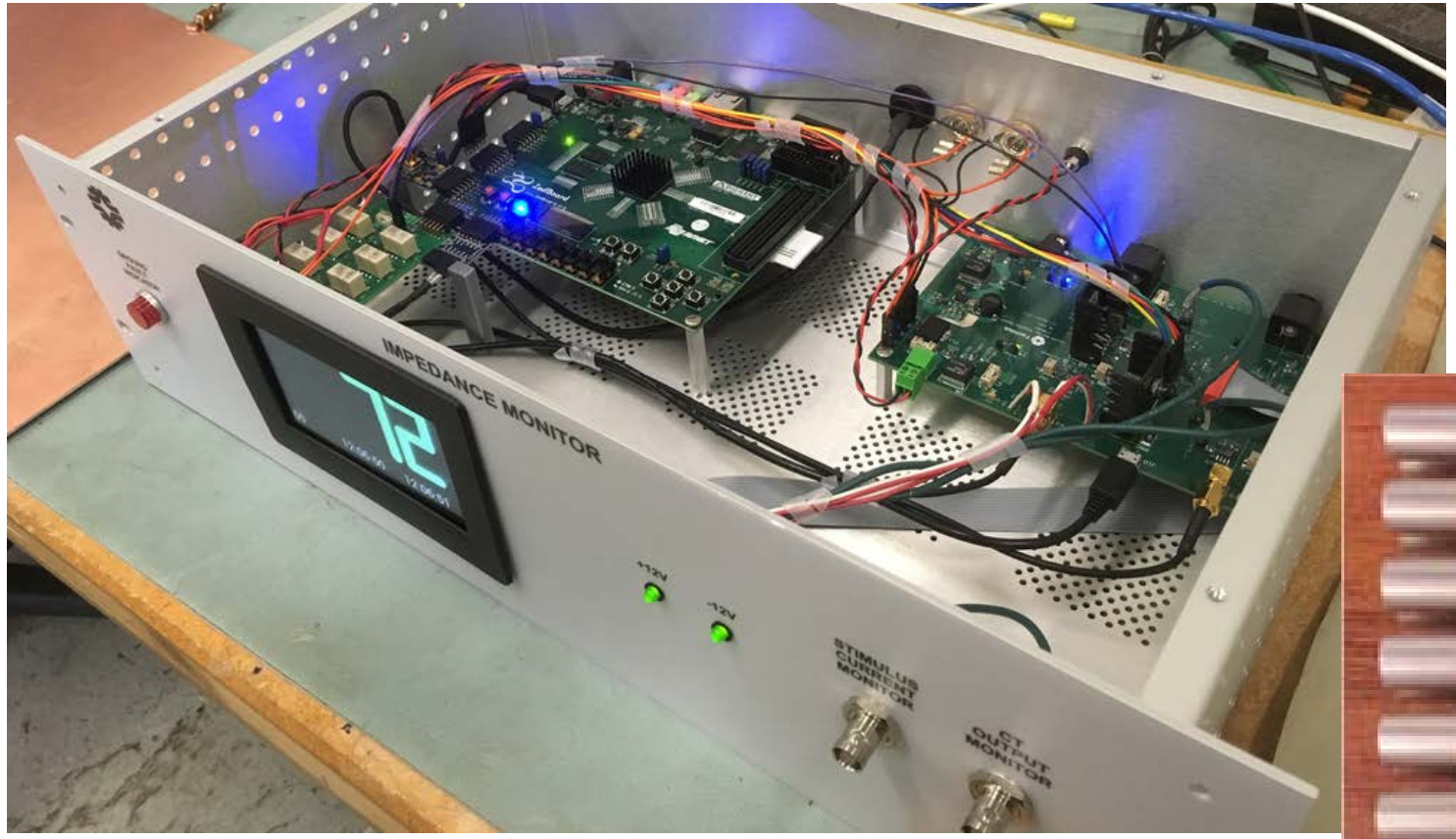
Right: next generation Pulsar3a prototype in Altium Designer.



Mike Utes

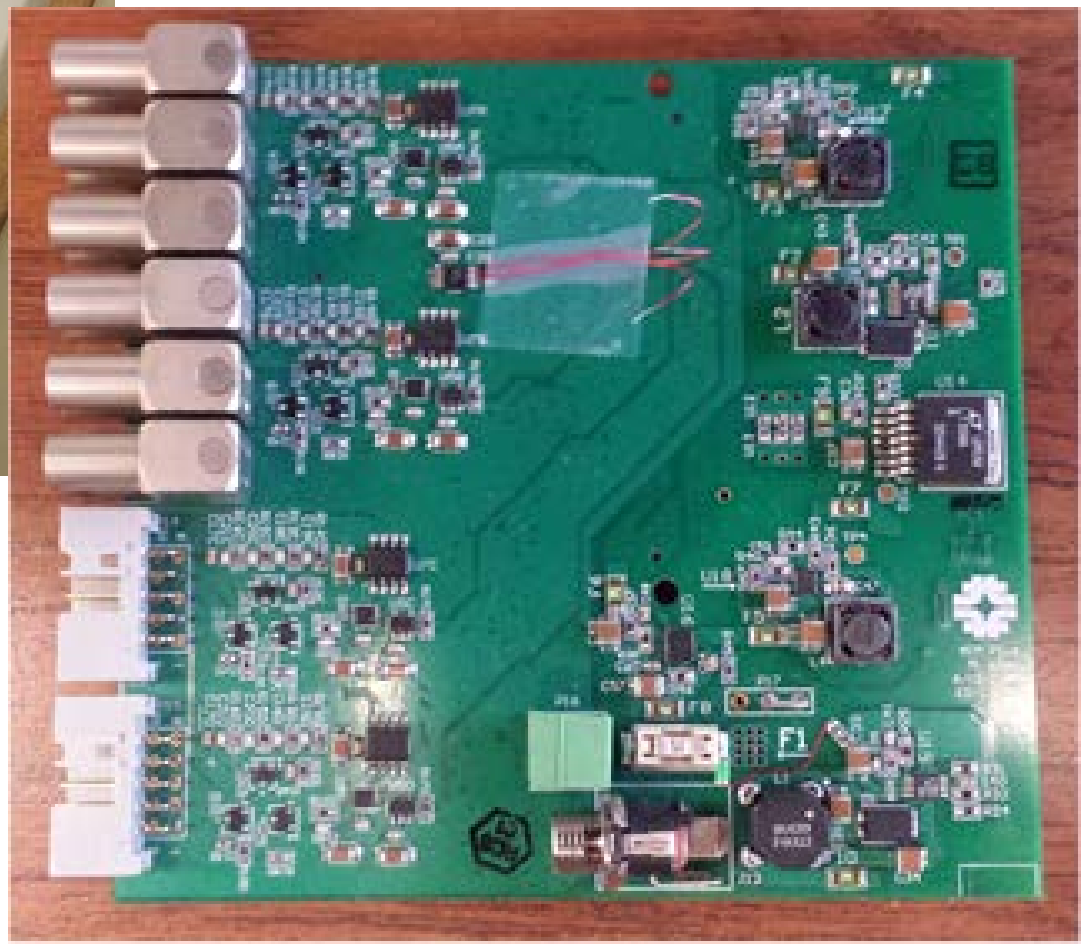
- Silicon Muon Scanner with Ron Lipton
  - Taking cosmic ray data
  - Designing "Lidboard" with Nina in Altium
  - Getting ready to populate HDI boards to make four more layers
- NIM Plus – modern NIM module where each channel can have a programmable pulse width and delay
- Impedance Monitor – worked with Co-Op Rich Prokop last summer
- Deputy Chair, Electrical Safety Subcommittee



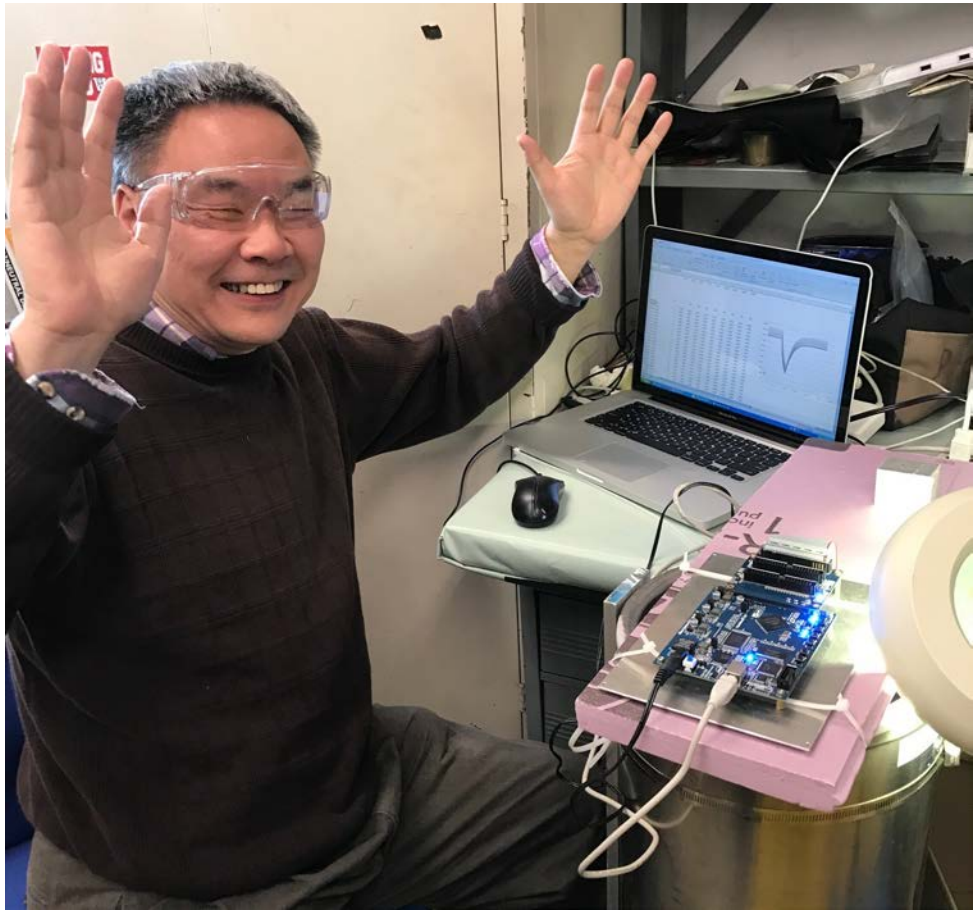


Impedance Monitor Chassis

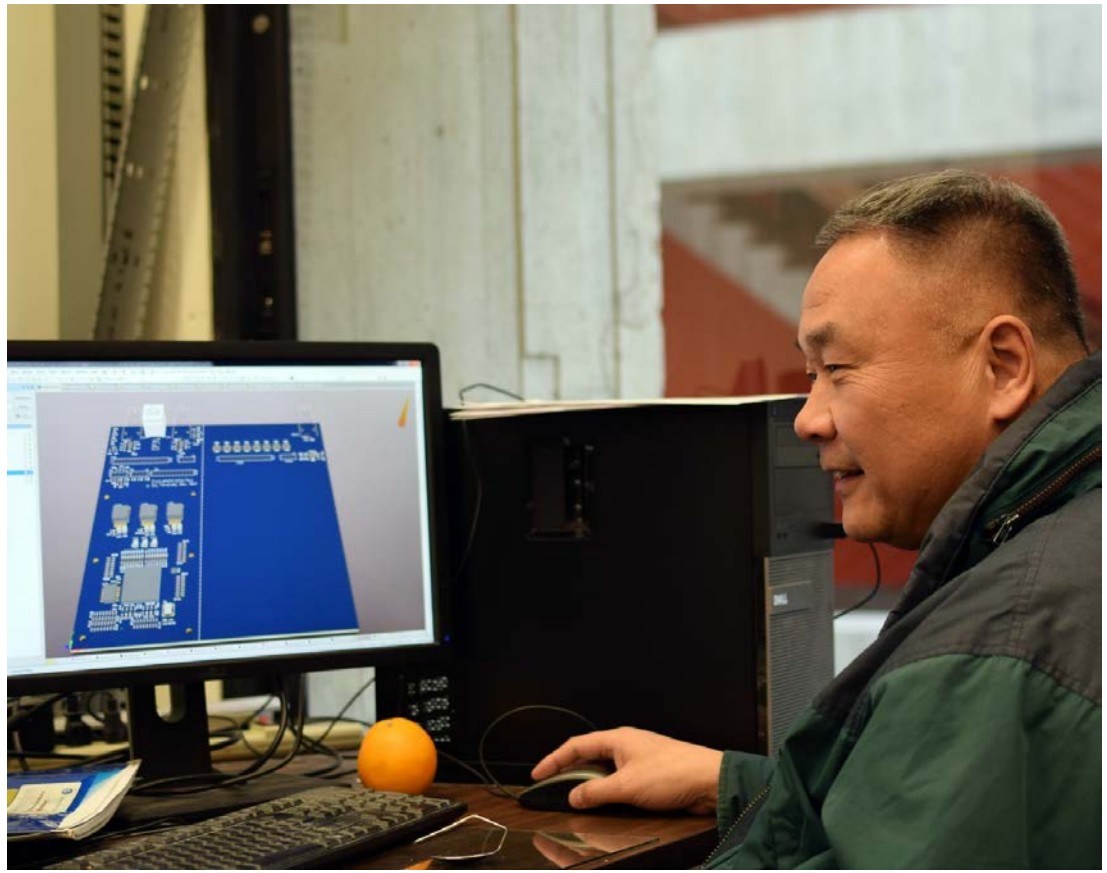
NIM Plus Board



Jin-Yuan Wu



Testing cold electronics for LAr detector.



Generic R&D using low cost FPGAs to implement high channel count precision TDC and ADC functions. Schematics and layout in Altium Designer

Co-Op Students

- Chris Edwards
  - NIU EE program
  - Junior, expected graduation May 2019
  - Working here during Spring and Fall Semesters 2018
  - Will continue working with Jamieson on Pulsar boards and firmware
- Rich Prokop
  - NIU EE program
  - Junior, expected graduation May 2019
  - Working here during Spring and Fall Semesters 2018
  - Will be working on the Silicon Muon Scanner with Mike Utes and Ron Lipton

ASIC Current Projects:

High Energy Physics

COLDATA: COLd DAta Transmission ASIC for DUNE **(CDP1 prototype under tests - OK)** **1.2 FTE**
Data transmission from cryostat to warm side at 1.2Gbps over up to 30m of Cu links and for control of Front-End and ADC chips, TSMC 65nm, cold models and digital libraries developed, collab. with SMU and BNL

COLD ADC: for DUNE **(started with LBL as lead, digital back-end Fermilab)** **2.5 FTE including testing**
12b, 2Msps ADC for DUNE liquid Ar TPC, pipeline with auto-calibration, TSMC 65nm, collab. with LBL, BNL

FanTastIC: Fast Timing Integrated Circuit for CMS EndCapTiming Layer **(start)** **1.5 FTE**
4×24 pixel RO IC providing ~20ps resolution for 1×3 mm^2 pixel LGAD sensors, collab. w. SLAC?, UCSC?

ECON: Endcap CONcentrator HGC Data Concentrator for CMS **(start)** **2 FTE**
64×1.28Gbps $\rightarrow$ 4×10Gbps tranceiver for trigger data and event data readout, TSMC 65nm, collab. w. CERN

RD53: CMS/ATLAS pixels +TSMC65nm standard cells with radiation models + TMR **<<1 FTE**

VIPRAM: Vertically-Integrated Pattern Recognition Associate Memory **(in fab.)** **<<1 FTE**
3D-integ. hardware tracking for Phase 2 CMS Upgrade, VIPRAM_3D and _L1CMS, GF 130nm, collab. NWU

FCP130/iFCP65: Fermilab CMS Pixels in 130 and 65nm **(testing of FCP130B)** **<<1 FTE**
Pixels for CMS Phase2 Upgrade + CERN RD53A in TSMC 65nm, collab. Univ. of Bergamo Italy (iFCP), KA25

Photon Science / WFO

VIPIC-L: Vertically-Integrated Photon Imaging Chip – Large **(in fab.)** **0.4 FTE (mainly testing)**
Fully 3D-integrated,1.2M pixel camera for X-ray Photon Correlation Spectroscopy, 8-12 keV X-rays, 0.7Tbs of data, wafer stacking moved Novati, TX $\rightarrow$ NCFab, NC, DOE-BES (FWP #FNAL 14-16), collab. with BNL, ANL

FLORA: Fermilab-LCLS CMOS 3D-integRated with Autogain **(FLORA_V1 to submit now)** **1 FTE**
Soft 0.2-2 keV X-rays, high speed 10kfps, high dynamic range 10^3, 2M pixel camera for LCSL II, 2-year R&D funded by DOE-BES (FWP #FNAL 16-21), collab. Fermilab-SLAC, extremely good review at LDAC2017

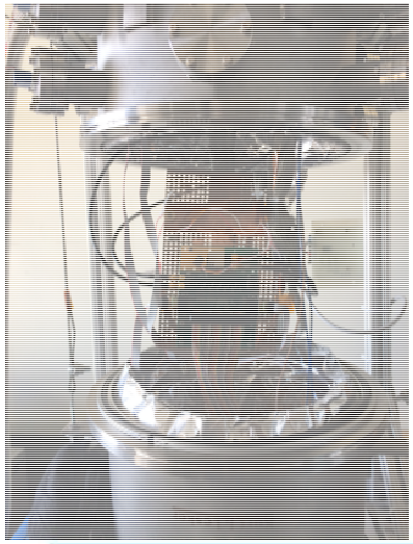
FASPAX $\rightarrow$ FAQIR: Fermi-Argonne Silicon Pixel Array X-ray **<<1 FTE (if phase II $\rightarrow$ 2 FTE)**
Extremely high dynamic range (up to 10^5 photons/pixel/pulse) pixel camera for 8-12 keV X-rays, (started as funded by APS-ANL Upgrade – SOW, now: Phase I commercialization SBIR grant with FieldViewers)

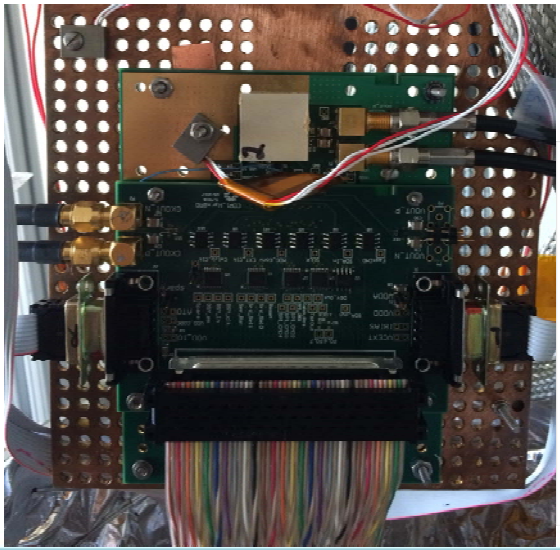
ASIC Current Projects:

COLDATA: COLd DAta Transmission ASIC for DUNE **(CDP1 prototype under tests - OK)** **1.2 FTE**
Data transmission from cryostat to warm side at 1.2Gbps over up to 30m of Cu links and for control of Front-End and ADC chips, TSMC 65nm, cold models and digital libraries developed, collab. with SMU and BNL

COLD ADC: for DUNE **(started with LBL as lead, digital back-end Fermilab)** **2.5 FTE including testing**
12b, 2Msps ADC for DUNE liquid Ar TPC, pipeline with auto-calibration, TSMC 65nm, collab. with LBL, BNL

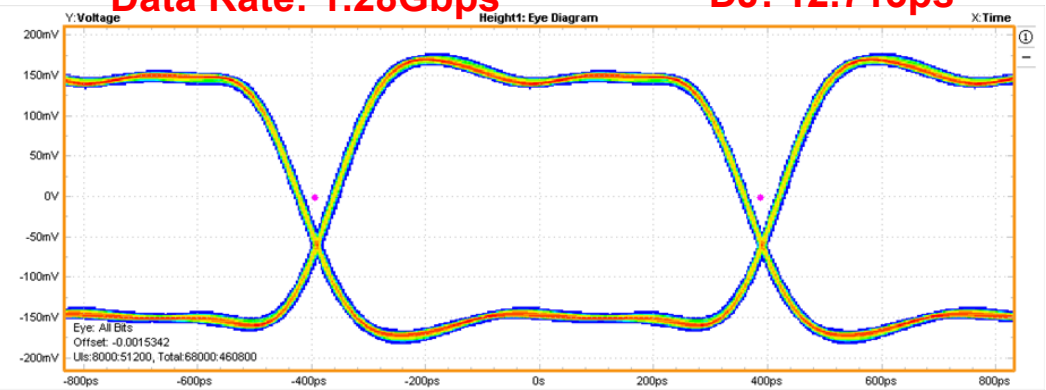
- ***Built library of standard cells based on modified transistor dimensions to meet lifetime requirements and characterize it using Cadence-Liberate for synthesis-place-route***
- ***Submitted prototype CDP1 ASIC in the TSMC 65nm process in May 2017 through CERN-IMEC Foundry Services using RD-53 agreement***
- ***Tests underway and show good operation of the chip both in RT and CT***





Temperature: 77K
Data Type: 1010
Data Rate: 1.28Gbps

Board#1：
TJ: 21.229ps
RJ: 0.599ps
DJ: 12.713ps

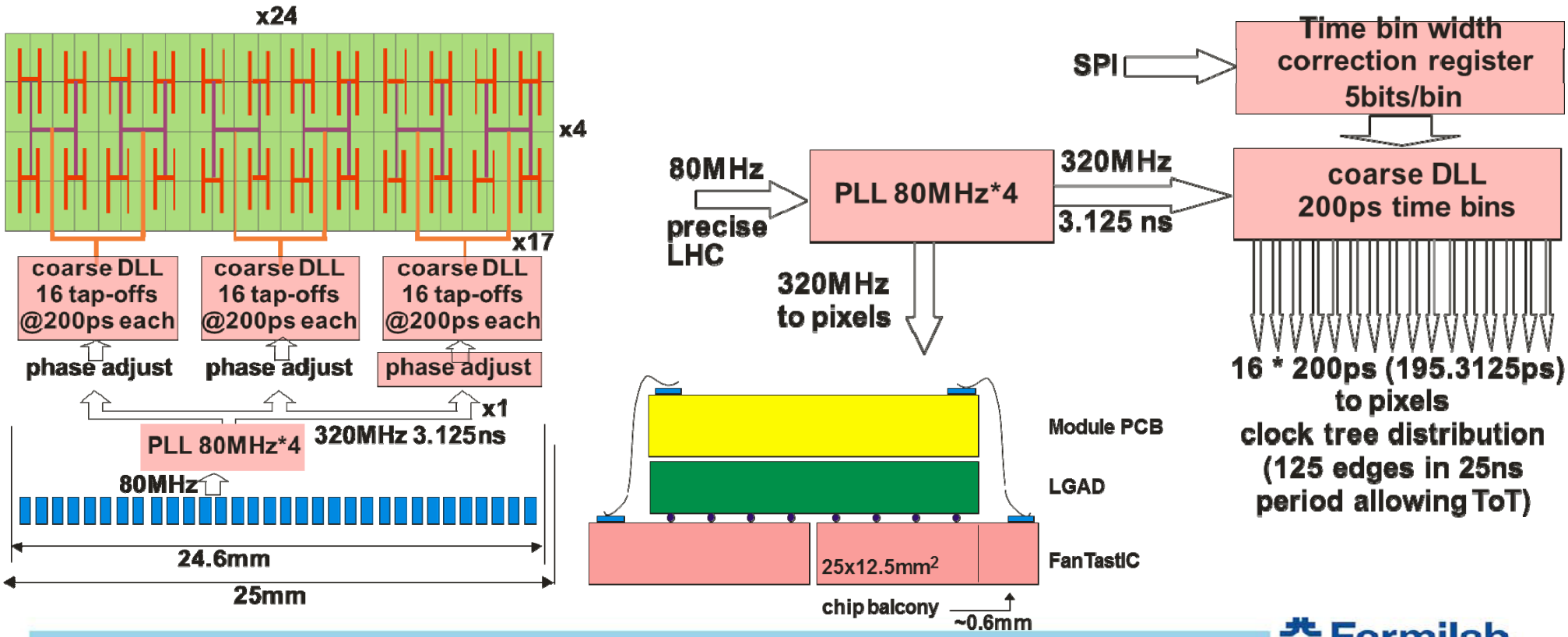


ASIC Current Projects:

FanTastIC: Fast Timing Integrated Circuit for CMS EndCapTiming Layer (start) 1.5 FTE

4 × 24 pixel RO IC providing ~20ps resolution for 1 × 3 mm² pixel LGAD sensors, collab. w. SLAC?, UCSC?

- ***Working on architecture of the first timing readout chip to be developed in the ASIC Group***
- ***Started specifying and design of main functional blocks***

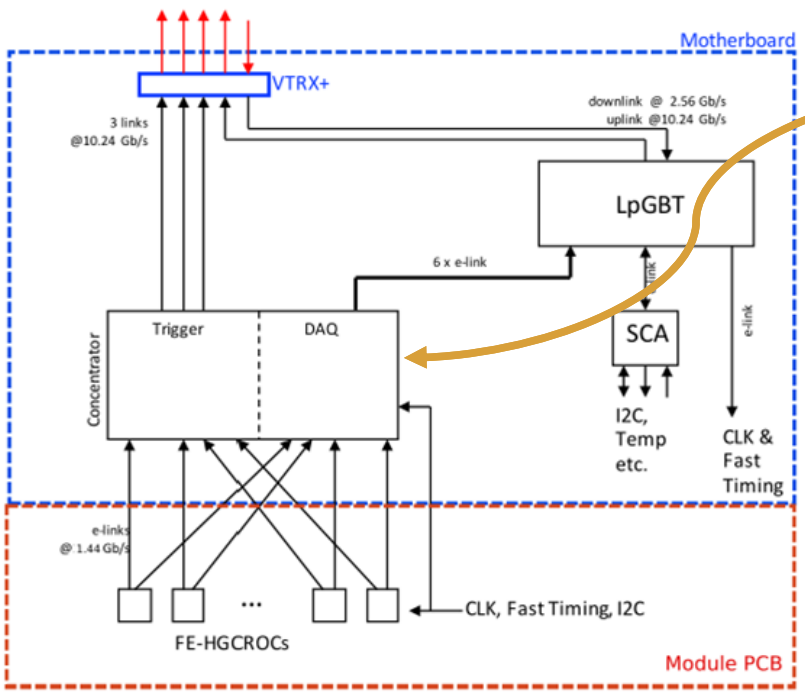


ASIC Current Projects:

ECON: Endcap CONcentrator HGC Data Concentrator for CMS (start) 2 FTE

64 × 1.28Gbps → 4 × 10Gbps tranceiver for trigger data and event data readout, TSMC 65nm, collab. w. CERN

- ***Working on architecture of the first massive data transfer chip with links at 10Gbps***
- ***Specification of the first prototype got accepted by the HGC group and is presented to USCMS***

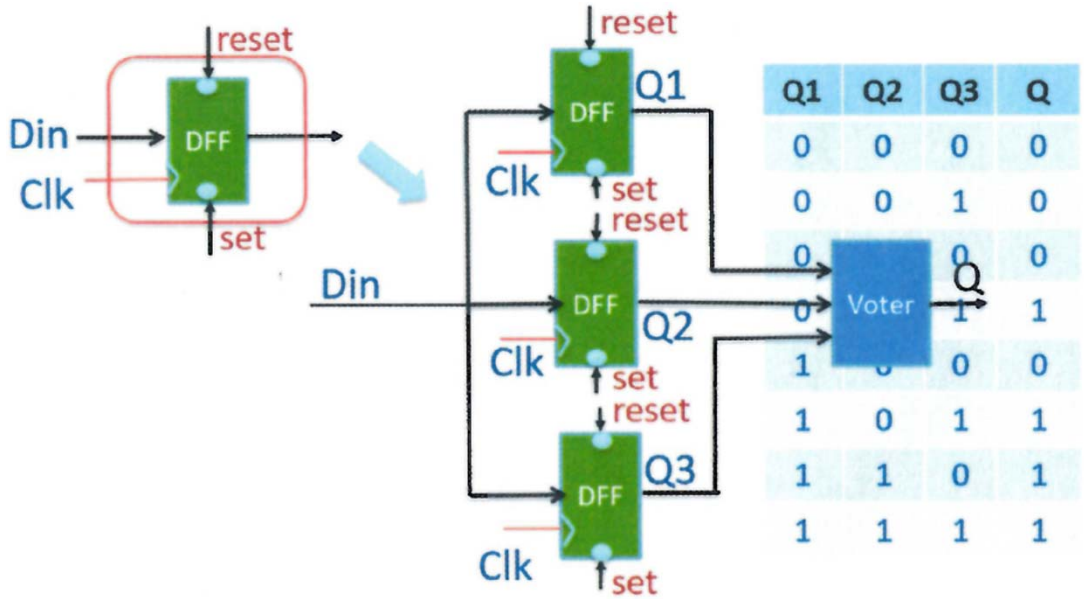


The Endcap Concentrator or ECON chip is responsible for acquiring data from a variable number of HGCROC front end chips, packing that data into frames and passing it off of the detector at high speed. It actually serves two independent data paths, the Trigger Path and the DAQ Path.

ASIC Current Projects:

RD53: CMS/ATLAS pixels +TSMC65nm standard cells with radiation models + TMR **<<1 FTE**

- ***Contribution to RD53A prototype through characterization of standard cells of dedicated layout with radiation models using Cadence Liberate***
- ***Development of Triple-Modular Redundant methodology for building SEE-hardened registers using the Cadence Genius/Innovus flow***
- ***Submission of LDRD proposal for FY2018/2019***



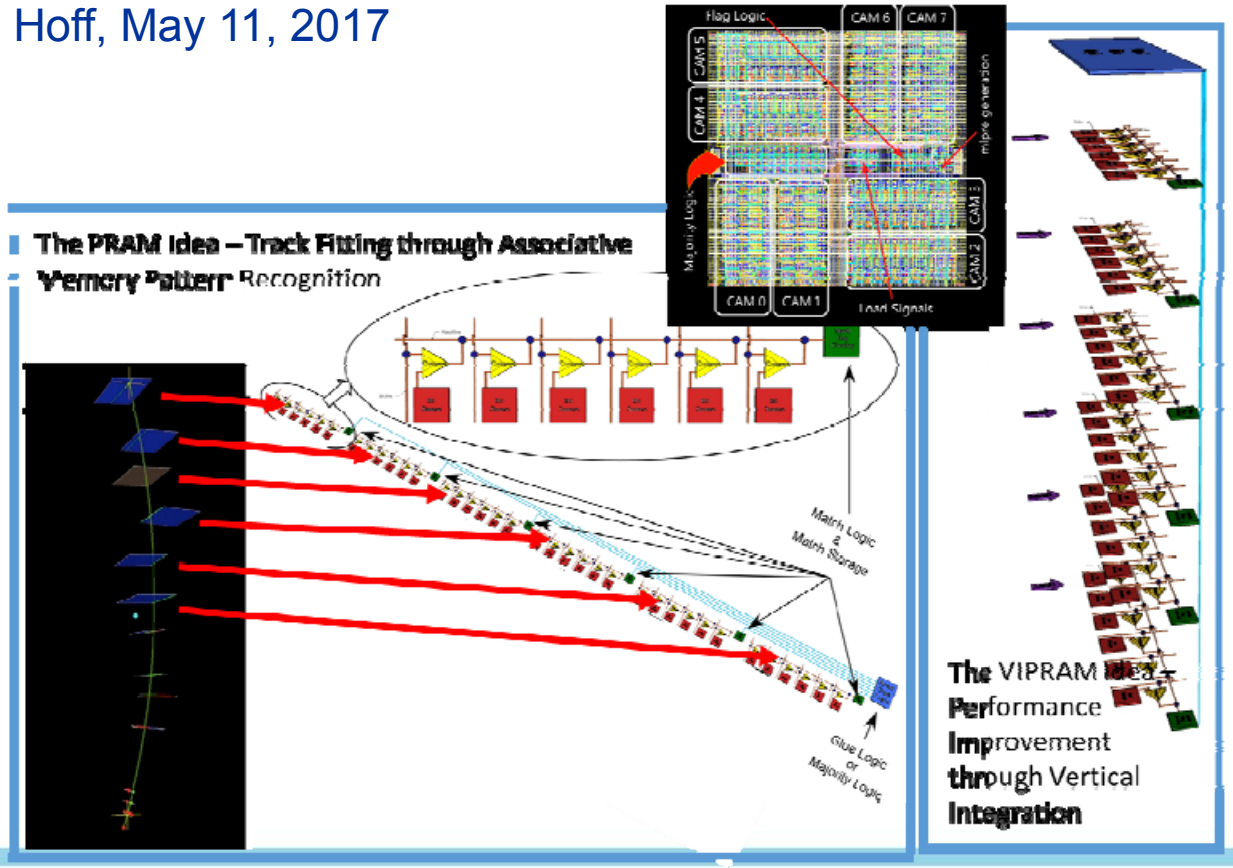
Q1	Q2	Q3	Q
0	0	0	0
0	0	1	0
0	[illegible]	0	0
0	[illegible]	1	1
1	[illegible]	0	0
1	0	1	1
1	1	0	1
1	1	1	1

ASIC Current Projects:

VIPRAM: Vertically-Integrated Pattern Recognition Associate Memory (in fab.) <<1 FTE

3D-integ. hardware tracking for Phase 2 CMS Upgrade, VIPRAM_3D and _L1CMS, GF 130nm, collab. NWU

- ***3D run is still in fab, 3D processing was moved from Novati Austin TX to North Carolina Fab Morrisville NC***
- ***Patent:* WO 2017039781 A3: Method and system for high performance real time pattern recognition,** J. Olsen, T. Liu, J. Hoff, May 11, 2017

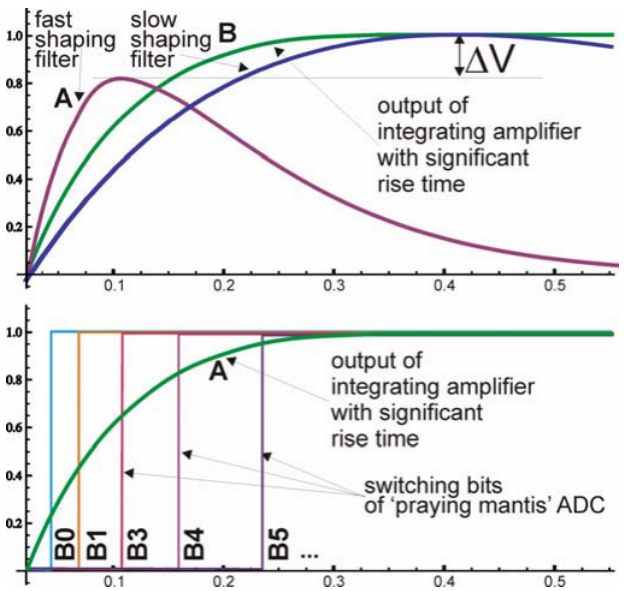


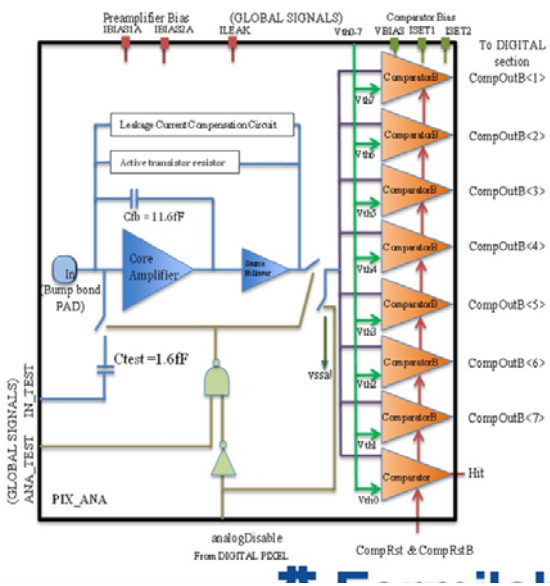
ASIC Current Projects:

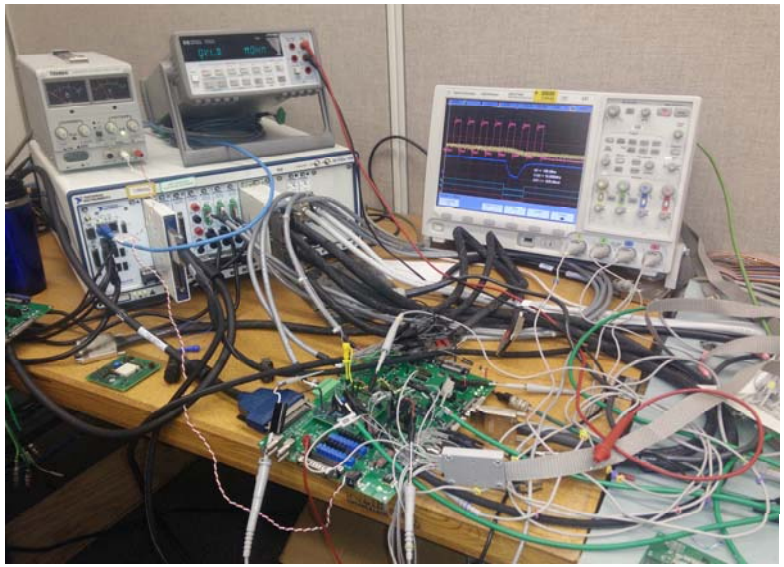
FCP130/iFCP65: Fermilab CMS Pixels in 130 and 65nm (testing of FCP130B) <<1 FTE

Pixels for CMS Phase2 Upgrade + CERN RD53A in TSMC 65nm, collab. Univ. of Bergamo Italy (iFCP), KA25

- ***FCP130 (version 2) under tests… shows signs of good operation especially… when BXClk is applied***
- ***Demonstration of leakage current compensation alternative to Krummenacher***
- ***FCP 130 may be a candidate for fast X-ray detection required at the MARIE facility at LANL (required 100Mfps X-ray detector)***
- ***Patent:* Time-Division Multiplexing Data Bus,** J. Hoff, submitted April 21 2016





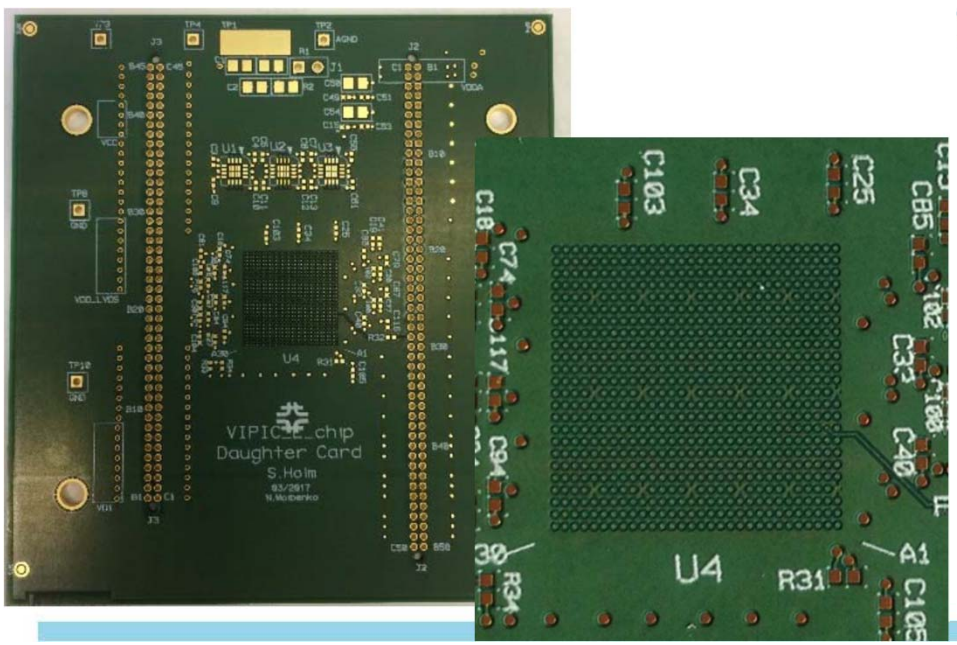


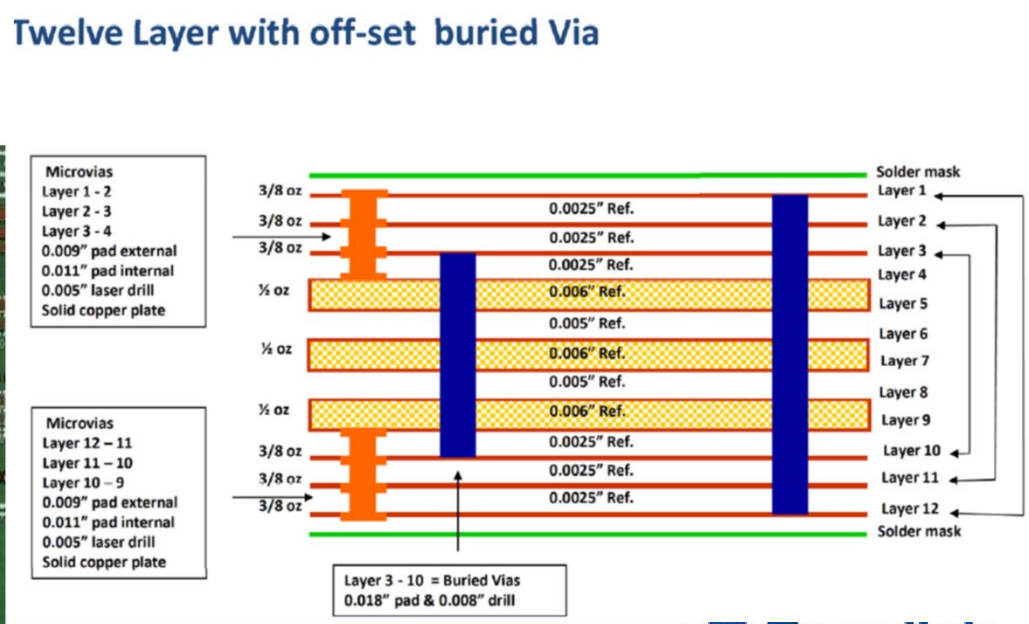
ASIC Current Projects:

VIPIC-L: Vertically-Integrated Photon Imaging Chip – Large (in fab.) **0.4 FTE (mainly testing)**

Fully 3D-integrated,1.2M pixel camera for X-ray Photon Correlation Spectroscopy, 8-12 keV X-rays, 0.7Tbs of data, wafer stacking moved Novati, TX → NCFab, NC, DOE-BES (FWP #FNAL 14-16), collab. with BNL, ANL

- ***3D run is still in fab, 3D processing was moved from Novati Austin TX to North Carolina Fab Morrisville NC (alternative with MIT-LL)***
- ***Preparation of tests: PCB 12 layers with 100um diameter microvias for 720 bump-bonds on the VIPIC-L chip at ~500um pitch***
- ***Patent:*** **Edgeless Large Area Camera System,** F. Fahim, G. Deptuch and VIPIC-L collab., submitted July 21 2016, under examination and **Edless Large Area ASIC ,** F. Fahim, G. Deptuch, submitted July 21 2016





ASIC Current Projects:

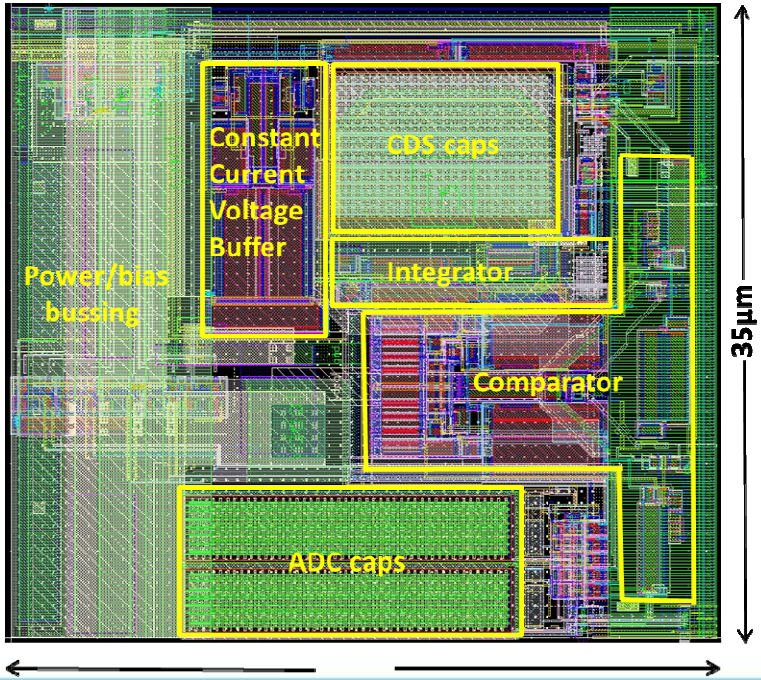
FLORA: Fermilab-LCLS CMOS 3D-integRated with Autogain (FLORA_V1 to submit now) 1 FTE

Soft 0.2-2 keV X-rays, high speed 10kfps, high dynamic range 10^3, 2M pixel camera for LCSL II, 2-year R&D funded by DOE-BES (FWP #FNAL 16-21), collab. Fermilab-SLAC,

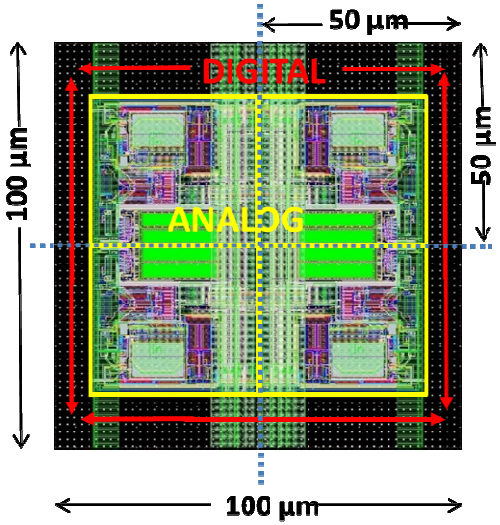
- ***Submission of FLORA_1 ASIC in January 2018 (first pixel detector with 10b-ADC/pixel and >10kfps readout)***
- ***Fabrication of passive and active MAPS sensors underway***
- ***Project received extremely good review at the LDAC review September 2017***

Pixel layout: one pixel (analog + digital) is 50 x 50 μm^2
Majority of the area occupied by analog functionality

One pixel (analog portion only)



4 pixels, mirrored vertically and horizontally forming 4 pixel island.



ASIC Current Projects:

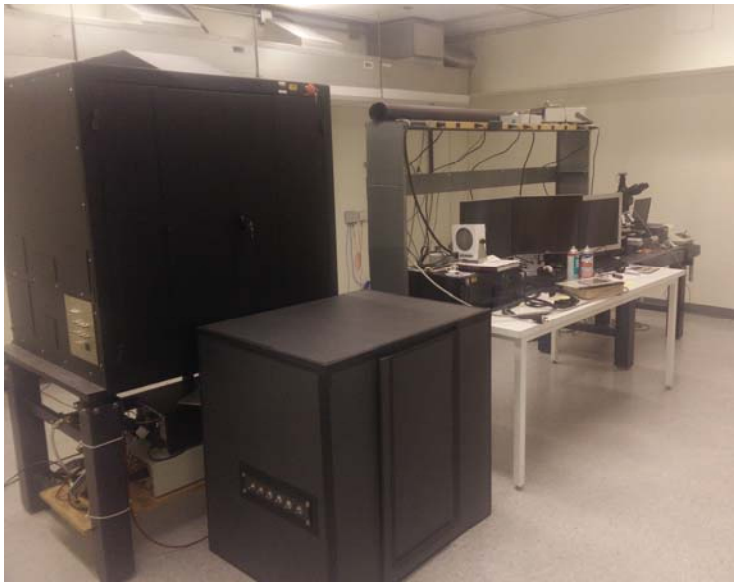
FASPAX → FAQIR: Fermi-Argonne Silicon Pixel Array X-ray **<<1 FTE (if phase II → 2 FTE)**

Extremely high dynamic range (up to 10^5 photons/pixel/pulse) pixel camera for 8-12 keV X-rays, (started as funded by APS-ANL Upgrade – SOW, now: Phase I commercialization SBIR grant with FieldViewers)

- ***Funding of SBIR-phase1 commercialization obtained by FieldViewers (CRADA signed with technology licensing), but ANL cancel funding from APS-U***
- ***FASPAX_V1.5 submitted in March 2017 r.***
- ***Testing shows good operation***
- ***SBIR-phase1 report due beginning of January 2018, considering partnering with FieldViewers for submission of SBIR-phase2 commercialization proposal to build large scale readout ASIC and X-ray camera***
- ***In parallel:***
  - ***glass interposer work through SBIR-phase1 with CVInc. (CRADA signed)***
  - ***Submission of US-Japan funding proposal for silicon interposer (KEK and AIST)***
- ***Patent:***
  - **US 9,794,499 B2: Wafer Scale Pixelated Detector System,** F. Fahim, G. Deptuch, T. Zimmerman, Oct.17, 2017
  - **Wafer-Scale Pixelated Detector System (CIP), pending,** F. Fahim, G. Deptuch, T. Zimmerman, submitted May 26 2016

ASIC Assets:

- ***New hires***
  - ***Pamela Klebber –application physicist (starts Jan.2018)***
  - ***Opening for Senior ASIC Engineer***



- ***Infrastructure***
  - ***Cleaned and little refurbished "CleanRoom"***

- ***Plans in Infrastructure***
  - ***Upgrade of robotic ASIC tester***
  - ***Purchase of wafer dicing saw for up to 12" wafers and special/rework dicing***
  - ***Build X-ray irradiation/testing station with probe station and laser***
  - ***Purchase semiconductor measurement C/V, I/V, characterization station***
  - ***Invest in high speed and RF capabilities (tbd)***

ASIC Publications (3 years):

1. S.Joshi, D.Li, S.Ogrenci-Memik, G.Deptuch, J.Hoff, S.Jindariani, T.Liu, J.Olsen, N.Tran, “A content addressable memory with multi-Vdd scheme for low power tunable operation”, 2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS), 2017 pp. 401-404
2. P.Kmon, G.Deptuch, F.Fahim, P.Gryboś, P.Maj, R.Szczygieł, T.Zimmerman, “Design of Analog Pixel Front-End for VIPIC-Large Detector”, IEEE Transaction on Circuits and Systems I: Regular Papers, vol. X, no. X, (XXX), pp. XXXX-YYYY
3. P.Otfinowski, G.Deptuch, P.Maj, “An Algorithm for Asynchronous Approximation of a Center of Gravity of Binary Objects”, IEEE Journal of Solid State Circuits, vol. X, no. X, (XXX), pp. X-Y
4. G.W.Deptuch, F.Fahim, P.Gryboś, J.Hoff, S.Holm, P.Maj, D.P.Siddons, P.Kmon, M.Trimpl, T.Zimmerman, “An Algorithm of an X-ray Hit Allocation to a Single Pixel in a Cluster and Its Test-Circuit Implementation”, IEEE Transaction on Circuits and Systems I: Regular Papers, vol. X, no. X, (XXX), pp. XXXX-YYYY
5. P.Otfinowski, P.Maj, G.Deptuch, F.Fahim, J.Hoff, “Comparison of Allocation Algorithms for Unambiguous Registration of Hits in Presence of Charge Sharing in Pixel Detectors“, 2017 JINST 12 C C01027
6. A.Krzyżanowska, G.Deptuch, P.Maj, P.Gryboś, R.Szczygieł, “Simulation approach to Charge Sharing Compensation Algorithms with experimental cross-check”, 2017 JINST 12 C03071
7. A.Krzyżanowska, G.Deptuch, P.Maj, P.Gryboś, R.Szczygieł, “Characterization of the Photon Counting CHASE Jr. Chip Built in a 40nm CMOS Process with the Charge Sharing Correction Algorithm Using a Collimated X-ray Beam”, IEEE Transaction on Nuclear Science, vol. 64, no. 9, (2017), pp. 2561-2568
8. Q.Zhang, E.M.Dufresne, P.Grybos, P.Kmon, P.Maj, S.Narayanan, G.W.Deptuch, R.Szczygiel, A.Sandy, “Submillisecond X-ray photon correlation spectroscopy from a pixel array detector with fast dual gating and no readout dead-time“, J. Synchrotron Radiat. 23 (2016) no.3, pp. 679-684
9. A.K.Rumaiz, D.P.Siddons, G.Deptuch, P.Maj, A.J.Kuczewski, G.A.Carini, S.Narayanan, E.M.Dufresne, A.Sandy, R.Bradford, A.Fluerasu and M. Sutton, “First experimental feasibility study of VIPIC: a custom-made detector for X-ray speckle measurements“, J. Synchrotron Radiat. 23, (2016), pp. 404-409
10. F.Fahim, G.W.Deptuch, J.R.Hoff, H.Mohseni, “Modeling and analysis of hybrid pixel detector deficiencies for scientific applications“, in SPIE Proceedings, Vol. 9555: Optical Sensing, Imaging, and Photon Counting: Nanostructured Devices and Applications, September 2015
11. F.Fahim, G.W.Deptuch, J.R.Hoff, H.Mohseni, “Design methodology: edgeless 3D ASICs with complex in-pixel processing for pixel detectors“, in SPIE Proceedings Volume 9555: Optical Sensing, Imaging, and Photon Counting: Nanostructured Devices and Applications, September 2015
12. G.W.Deptuch, G.Carini, P.Enquist, P.Gryboś, S.Holm, R.Lipton, P.Maj, R.Patti, D.P.Siddons, R.Szczygieł, R.Yarema, “Fully 3D-integrated Pixel Detectors for X-Rays“, IEEE Transaction on Electron Devices, vol. 63, no. 1, (2016), pp. 205-214
13. J.Hoff, G.W.Deptuch, F.Fahim, P.Gryboś, P.Maj, Member, D.P.Siddons, R.Szczygieł, M. Trimpl, T.Zimmerman, “An on-Chip Charge Cluster Reconstruction Technique in the miniVIPIC Pixel Readout Chip for X-ray Counting and Timing”, in Proceeding of 2014 IEEE Nuclear Science Symposium Conference Record, 2014, Seattle, WA, USA,. FERMILAB-CONF-14-528-PPD
14. J.R.Hoff, G.W.Deptuch, G.Wu, P.Gui, “Cryogenic Lifetime Studies of 130 nm and 65 nm nMOS Transistors for High-Energy Physics Experiments”, IEEE Transaction on Nuclear Science, vol. 62, no. 3, (2015), pp. 1255-1261
15. G.W.Deptuch, G.Carini, T.Collier, P.Gryboś, P.Kmon, R.Lipton, P.Maj, M.Trimpl, D.P.Siddons, R.Szczygieł, R.Yarema, “Results of Tests of Three-Dimensionally Integrated Chips Bonded to Sensors”, IEEE Transaction on Nuclear Science, vol. 62, no. 1, (2015), pp. 349-358
16. P.Maj, P.Grybos, R.Szczygiel, P.Kmon, R.Kłeczek, A. Drozd, P.Otfinowski, G.Deptuch, “Measurements of Matching and Noise Performance of a Prototype Readout Chip in 40 nm CMOS Process for Hybrid Pixel Detectors”, IEEE Transaction on Nuclear Science, vol. 62, no. 1, (2015), pp. 359-367
17. L.Altman, G.Carini, G.Deptuch, F.Fahim, P.Grybos, U.Heintz, J.Hoff, S.Holm, R.Lipton, M. Narain, S.Poprocki, A.Shenai, P.Siddons, R.Syarif, R.Szczygiel, J.Thom, M.Trimpl, M.Tripathi, P.Wittich, R.Yarema, Z.Ye, T.Zimmerman, “Three Dimensional Integrated Circuits Bonded to Sensors”, PoS(VERTEX2014)045
18. J.Thom, R.Lipton, U.Heintz, M.Johnson, M.Narain, R.Badman, L.Spiegel, M.Triphati, G.Deptuch, C.Kenney, S.Parker, Z.Ye, D.P.Siddons, “3D IC for future HEP detectors“, 2014 JINST 9 C11005
19. P.Maj, P.Gryboś, R.Szczygieł, P.Kmon, A.Drozd, G.Deptuch, “A pixel readout chip in 40 nm CMOS process for high count rate imaging systems with minimization of charge sharing effects” 2013 IEEE Nuclear Science Symposium Conference Record, 2013, Seoul, South Korea
20. R.Yarema, G.Deptuch, R.Lipton, “Recent Results for 3D Pixel Integrated Circuits Using Copper-Copper and Oxide-Oxide Bonding“, PoS(VERTEX 2013)032
21. G.W.Deptuch, G.Carini, P.Gryboś, P.Kmon, P.Maj, M.Trimpl, D.P.Siddons, R.Szczygieł, R.Yarema, “Design and Tests of the Vertically Integrated Photon Imaging Chip”, IEEE Transaction on Nuclear Science, vol. 61, no. 1, (2014), pp. 663-674.
22. G.Wu, G.Deptuch, J.Hoff, P.Gui, “Degradations of threshold voltage, mobility and drain current and the dependence on transistor geometry for stressing at 77 K and 300 K“, IEEE Transactions on Device and Materials Reliability, vol.14, no.1, (2014), pp.477-483.
23. F.Fahim, G.Deptuch, S.Holm, A.Shenai, R.Lipton, “Monolithic Active Pixel Matrix with Binary Counters ASIC With Nested Wells”, 2013 JINST 8 C04008.
24. R.Yarema, G.Deptuch, J.Hoff, F.Khalid, R.Lipton, A.Shenai, M.Trimpl, T.Zimmerman, “Vertically Integrated Circuit Development at Fermilab for Detectors”, 2013 JINST 8 C01052.
25. R.Lipton, G.Deptuch, U.Heintz, M.Johnson, C.Kenney, M.Narian, S.Parker, I.Planell-Mendez, E.Sawyer, A.Shenai, L.Spiegel, J.Thom, Z.Ye, “Combining the Two 3Ds”, 2012 JINST 7 C12010.
26. P.Maj, A.Baumbaugh, G.Deptuch, P.Grybos, R.Szczygieł, “Algorithms for Minimization of Charge Sharing Effects in a Hybrid Pixel Detector Taking into Account Hardware Limitations in Deep Submicron Technology”, 2012 JINST 7 C12020.
27. T.Liu, J.Hoff, G.Deptuch, R.Yarema, “A New Concept of Vertically Integrated Pattern Recognition Associative Memory”, Physics Procedia, Vol. 37, 2012, pp. 1973-1982.
28. P.Maj, G.Carini, G.Deptuch, P.Grybos, P.Kmon, D.P.Siddons, R.Szczygiel, M.Trimpl, R.Yarema, “Tests of the First Three-Dimensionally Integrated Chip for Photon Science”, PoS(VERTEX 2012) (2013) 027 2.