Fermi National Accelerator Laboratory
Particle Physics Division

Mechanical Department Engineering Note

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Project: *CDF Run 2B Silicon*

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Title: ***Mechanical Evaluation of an Alternative Mini-Portcard Design Using a Polyimide-Based Substrate***

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Reviewer(s): ---

Key Words: *CDF / Silicon*

Abstract/Summary:

It has been suggested by the electrical engineering group on the CDF SVX Run 2B project that the beryllia mini-portcards (miniPCs), which are very expensive, have very long lead times, and have a beryllium handling concern, could be replaced by a polyimide-based alternative design, which is inexpensive and quickly fabricated. In order to help evaluate the impact of this alternative design, several aspects of the mechanical design have been investigated:

Radiation Length:	The polyimide design has about half the radiation length of the beryllia design.
Thermal Performance:	The transceiver chips run significantly warmer for the polyimide design (about 18 vs. 6°C). However, the average temperature of the miniPC top surface is only about 2 or 3 °C warmer than that for the BeO design.
Stave Mechanics:	The polyimide design was found to generate increased thermal stave bowing (~50% increase) due to its high CTE relative to other stave materials.

Applicable Codes: *N/A*

RADIATION LENGTH

The BeO and polyimide MiniPC RL has been estimated by assuming that the substrate material is a homogeneous mixture spread out over a 20 cm^2 footprint (1.55 x 2.0 inches) and that the flux path is normal to the plane of the card. Surface mount components are assumed to be the same for each design and are therefore left out. Wing solder is included for the beryllia design since the polyimide design would likely have an integrated wing cable.

Material	**Description**	**Volume (mm^3)**	**Mass (g)**	**Matl. Xo (g/cm^2)**	**%RL**	**% of Total %RL**
Beryllia MiniPC Total = 3.7 grams / 1.23 %RL						
Substrate	BeO, 0.38 mm thick	760.0	2.166	41.31	0.26	21
Glass	SiO_2, 6 layers, 14 μm each	168.0	0.373	27.04	0.07	6
Gold (Trace)	3 layers, 30% coverage, 8 μm each	14.4	0.278	6.43	0.22	71
Gold (Power)	1 layer, 70% coverage, 8 μm each	11.2	0.216		0.17	
Gold (Ground)	2 layers, 100% coverage, 8 μm each	32.0	0.618		0.48	
Wing Solder	63/37 tin/lead	5.1	0.045	7.72	0.03	2
Polyimide MiniPC Total = 3.2 grams / 0.69 %RL						
Substrate	5 layers, 5 mils each	1270	1.803	38.4[1]	0.23	34
Kapton Covers	2 layers, 2 mils each	203.2	0.289	38.4	0.04	5
Copper (Trace)	2 layers, 30% coverage, 9 μm each	10.8	0.096	12.86	0.04	61
Copper (Trace)	1 layer, 30% coverage, 18 μm each	10.8	0.096		0.04	
Copper (Power)	1 layer, 70% coverage, 18 μm each	25.2	0.225		0.09	
Copper (Ground)	2 layers, 100% coverage, 18 μm each	72.0	0.643		0.25	

These results indicate that the polyimide miniPC has a much smaller radiation length than the BeO design.

[1] Kapton value assumed.

THERMAL ANALYSIS

The thermal comparison of the designs was analyzed by Mr. Masato Aoki. A report that documents the numerous cases investigated is included in the Appendix. All cases assumed the same stave core conditions (glue gaps, carbon fiber data, -15°C coolant temperature, etc.) and same ambient conditions (+5°C with h=3 W/m^{2}K)

For the BeO design, gold-filled thermal vias under the transceiver chips conduct heat through the dielectric layer down to the high-conductivity beryllia, which spreads the heat. Heat is then conducted through the bottom dielectric and the glue into the carbon fiber stave skin, where it is spread further. It is then conducted to the cooling tubes that run in two paths beneath the skin.

Both a nominal case and a case that assumes a 4 mm air bubble directly underneath a chip have been investigated. As the following results show, there is little difference between these two cases since the BeO is a pretty effective heat spreader.

BeO MiniPC	**Base Case**	**Air Bubble Case**
Max. Chip Temperature	5.7°C	5.9°C
Max. Substrate Top Surface Temperature	2.3	2.5
Min. Substrate Top Surface Temperature	-2.7	-2.5
Estimated Average Top Surface Temperature (including chip)	-0.4	-0.3

For the polyimide design, the initial design intent had been to use thermal vias to conduct the chip heat down to the digital ground layer, which would spread the heat. Copper layers were available in 9 or 18 μm thicknesses. Additional vias out along the edges of the card would then conduct heat from the digital ground down to the analog ground layer. This had to be done along the edges since the analog ground could not actually be electrically connected to digital ground – instead, areas for digital ground were to be preserved along the edge of the card. In this way, it was hoped that the heat would be spread over a larger area, thus aiding conduction.

Initial cases investigating different numbers of vias and different copper thicknesses resulted in maximum temperatures between about +20 and +40°C. Temperature distributions in the digital ground plane indicated that the heat was simply not spreading as hoped in this layer. Therefore, an alternative approach of putting islands of digital ground in the analog ground layer directly underneath the chips, with via towers linking them thermally, was investigated. This was a bit more promising, but was thought to be much more sensitive to the potential of an air bubble trapped underneath the via field position.

The results of a comparison case are shown below. These cases assume 6 vias underneath each chip with 1.5 mils of copper plated in a 10 mil hole. Improvements could be gained by

increasing the cross-section area of via copper by increasing their number or the plating thickness. Larger digital ground island size is also a benefit.

Polyimide MiniPC	**Base Case**	**Air Bubble Case**
Max. Chip Temperature	17.7°C	19.7°C
Max Substrate Top Surface Temperature	11.5	13.1
Min Substrate Top Surface Temperature	-4.0	-3.5
Estimated Average Top Surface Temperature (including chip)	1.6	2.4

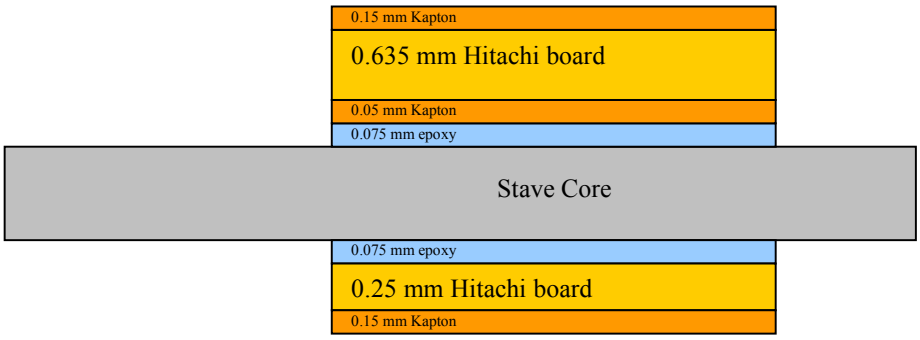
The results indicate that the chips run considerably warmer than the BeO cases, but certainly not above the temperature limit allowable for the chip itself. Although the chips may run notably hotter, the average temperature of the top surface is only 2 or 3 °C warmer than the BeO design.

STAVE MECHANICS

The change in miniPC material could also potentially have an impact on stave mechanics. Previous analyses of stave sag and thermal warpage with the beryllia design have been documented in CDF/DOC/SEC_VTX/PUBLIC/5869. The results of that study are shown below in Figure 2A (gravitational sag) and Figure 3A (gravitational sag + differential thermal expansion effect going from +20 to -15°C). Note that these analyses do not have a wing cable stiffener on the non-trigger side of the stave since this feature had not been fully developed at the time the analyses had been performed. The effect of this stiffener on stave mechanics is expected to be very small.

These same analyses have now been performed with the polyimide miniPC. The thicknesses assumed are shown in Figure 1 below. For the Hitachi substrate material, a CTE of 55 ppm/°C (from Hitachi polyimide MCL data sheet) and a modulus of 18.4 GPa (G10 value – no actual vendor information available) was assumed. Although the CTE is much higher than that for BeO, it is much less stiff.

Figure 1 – Structural Model Layout (Side View)



The room temperature sag results are shown in Figure 2B and were found to be the virtually identical to the beryllia results. This insignificant difference was expected since this card is small relative to the stave and it is located near one end.

The bigger difference is expected for the differential coefficient of thermal expansion analysis, since the miniPC region is the only area of the stave that is not symmetric. The results of this analysis are shown in Figure 3B and show that the polyimide case causes more warpage than the beryllia case (about 86 vs. 56 μm) due to its very high CTE, even though it is not as stiff as the BeO.

FIGURE 2A – Sag with BeO MiniPC

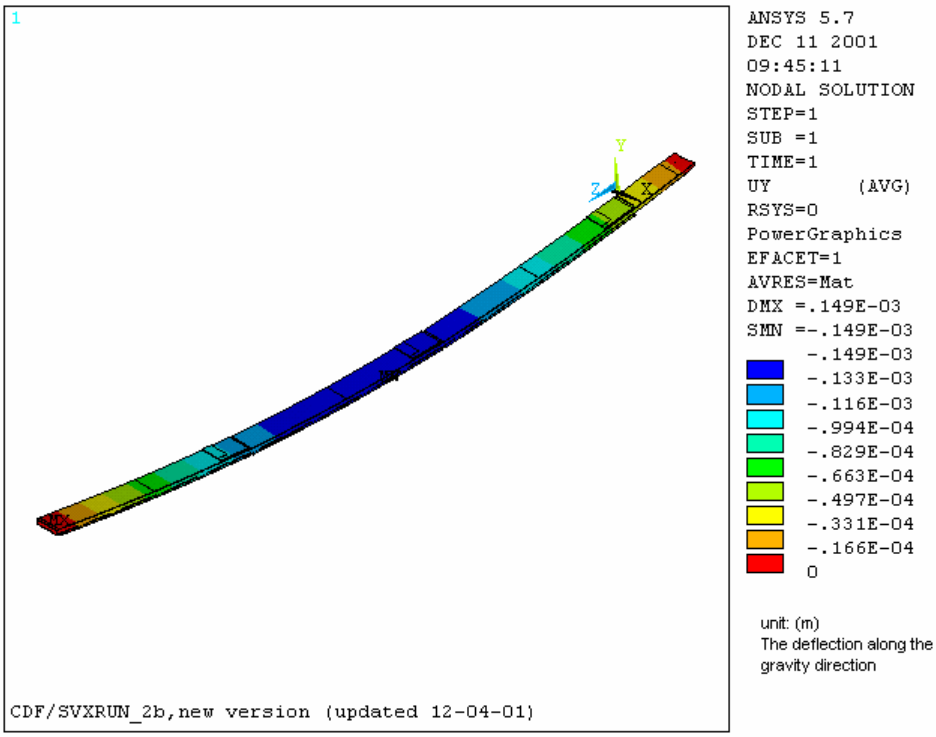


FIGURE 2B – Sag with Polyimide MiniPC

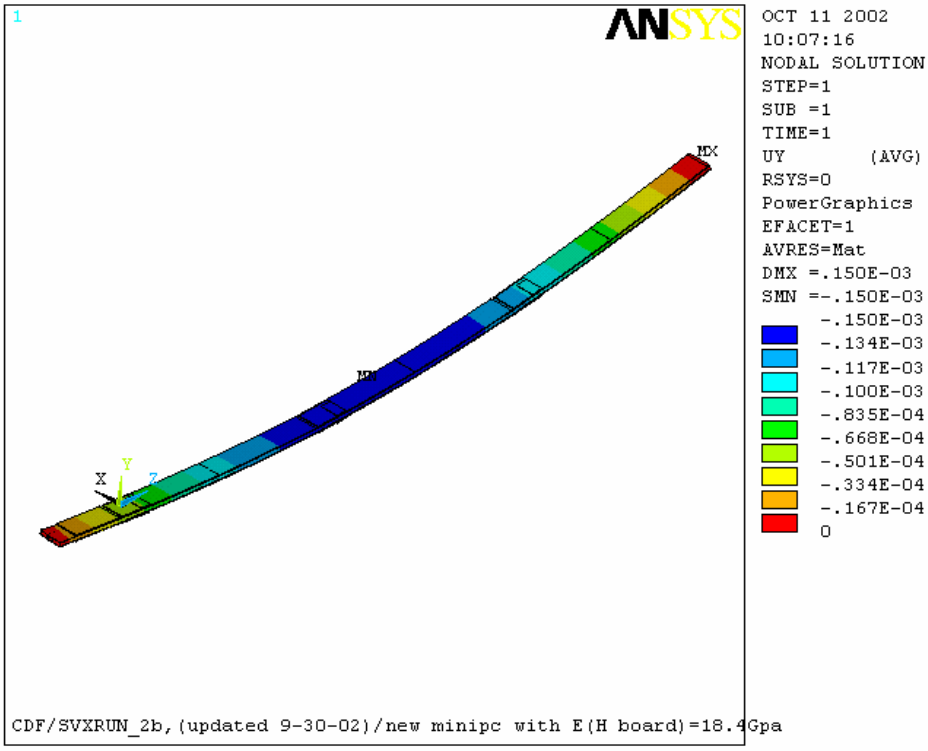


FIGURE 3A – Sag & Thermal Bow with BeO MiniPC

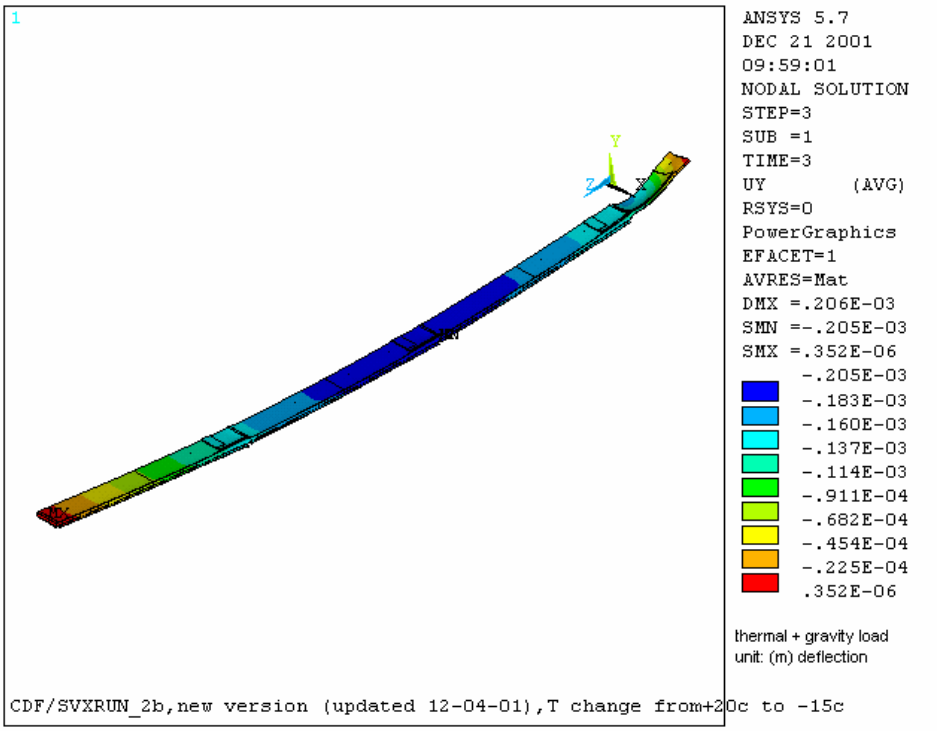
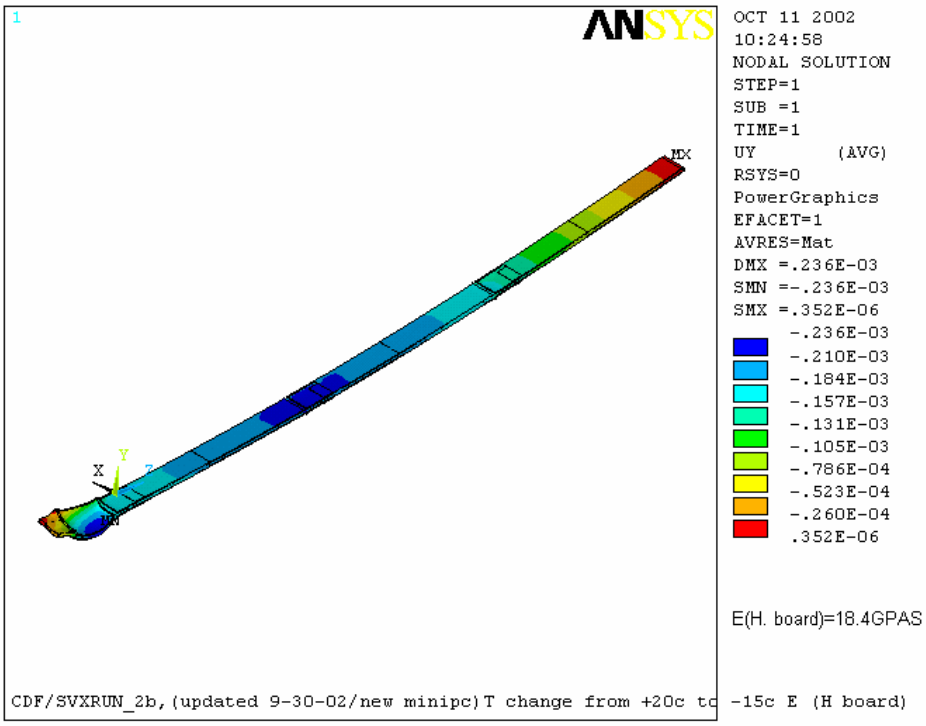


FIGURE 3B – Sag & Thermal Bow with Polyimide MiniPC



APPENDIX

Finite Element Analysis Thermal Comparison of Beryllia and Polyimide MiniPCs

Thermal Analysis Simulation about mini Port Card with ANSYS

Masato Aoki

Parameters

Temperature (degree C)

- Air = 5
- Coolant = -15

Heat transfer coefficient : h (W/m^2 k)

- Air = 3
- Coolant = 700

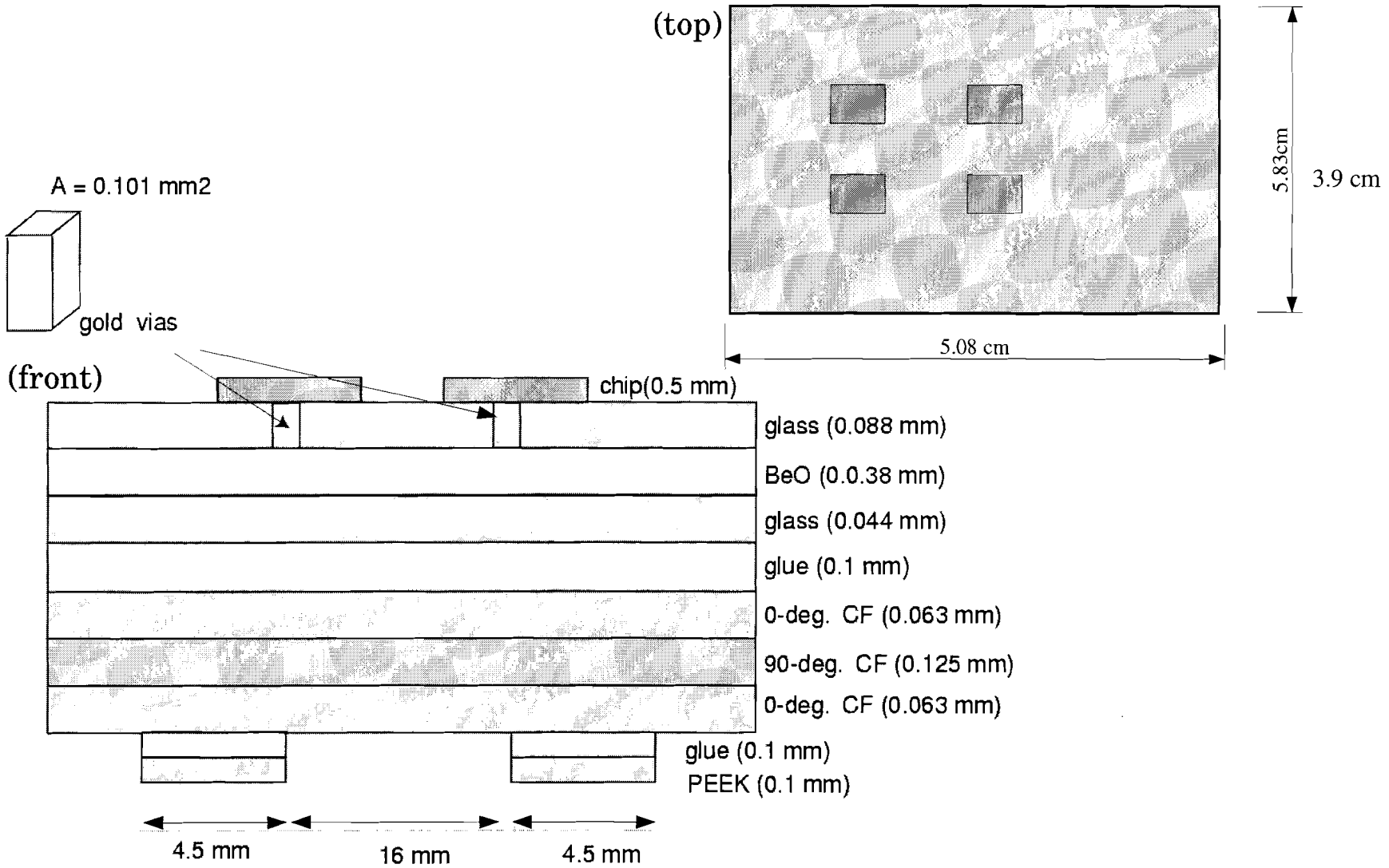
Thermal conductivity : k (W/m k)

- Silicon(chip) = 148
- Glass = 1.0
- Gold = 317
- Copper = 401
- BeO = 248
- Glue = 0.1
- Carbon Fiber = 372(0 deg.) / 1(90 deg.)
- PEEK = 0.25
- Polyimide = 0.12

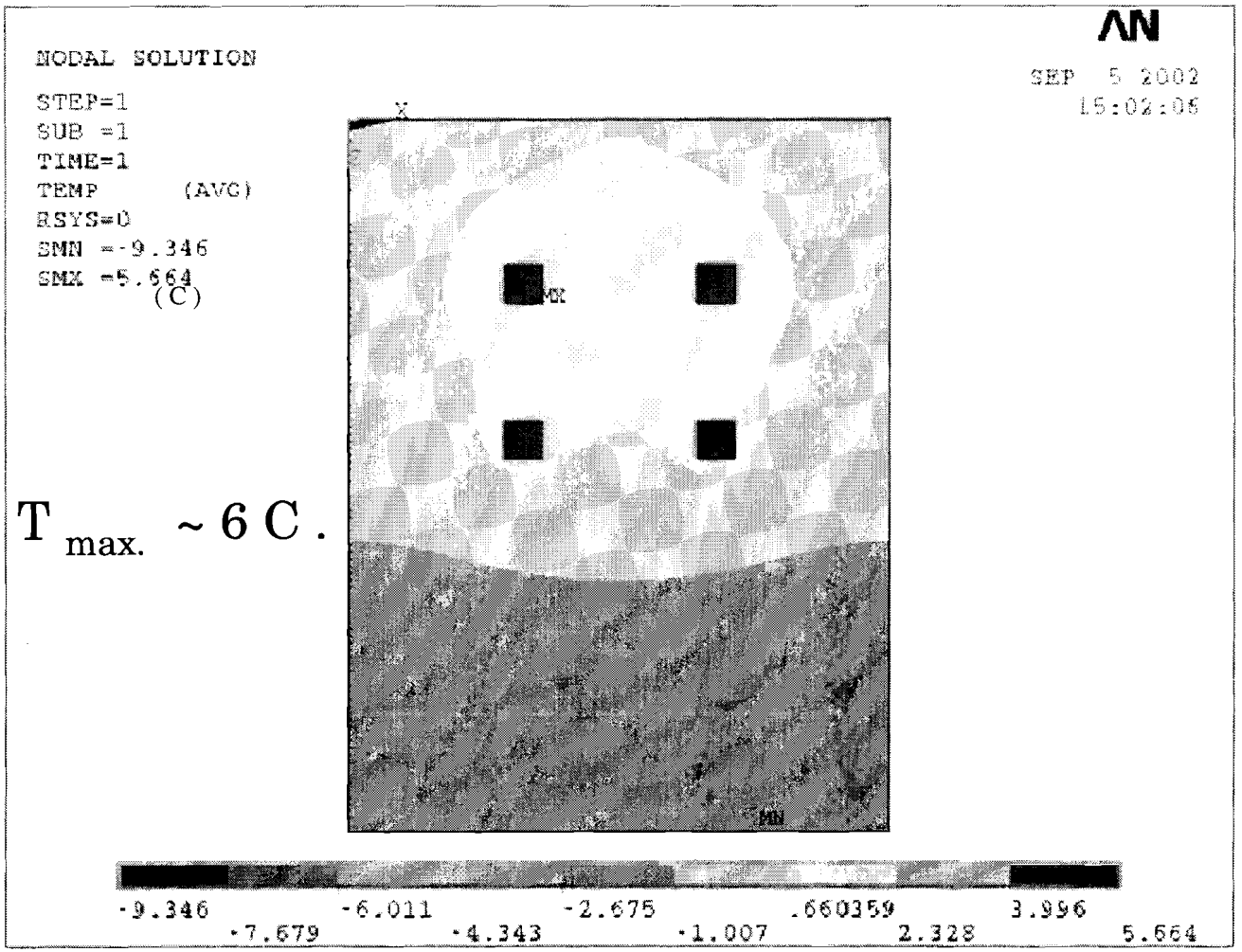
Heat rate

0.5 W/chip

Geometry of BeO miniPC used in this simulation

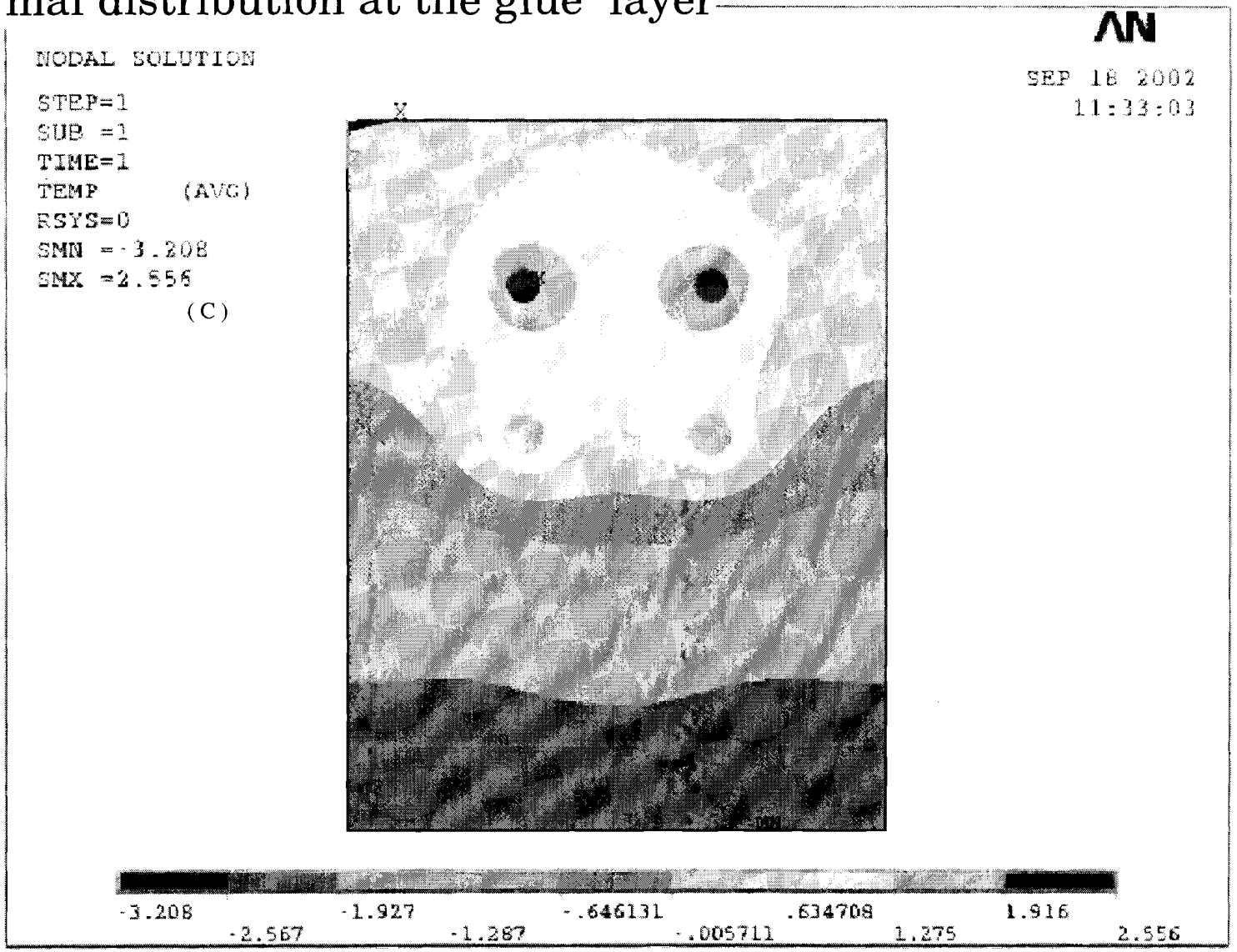


Thermal distribution of BeO miniPC



$T_{max.} \sim 6\ C$.

Thermal distribution at the glue layer



Modifying the thermal conductivity of gold vias

Measured thermal conductivity is usually less than the pure metal conductivity.

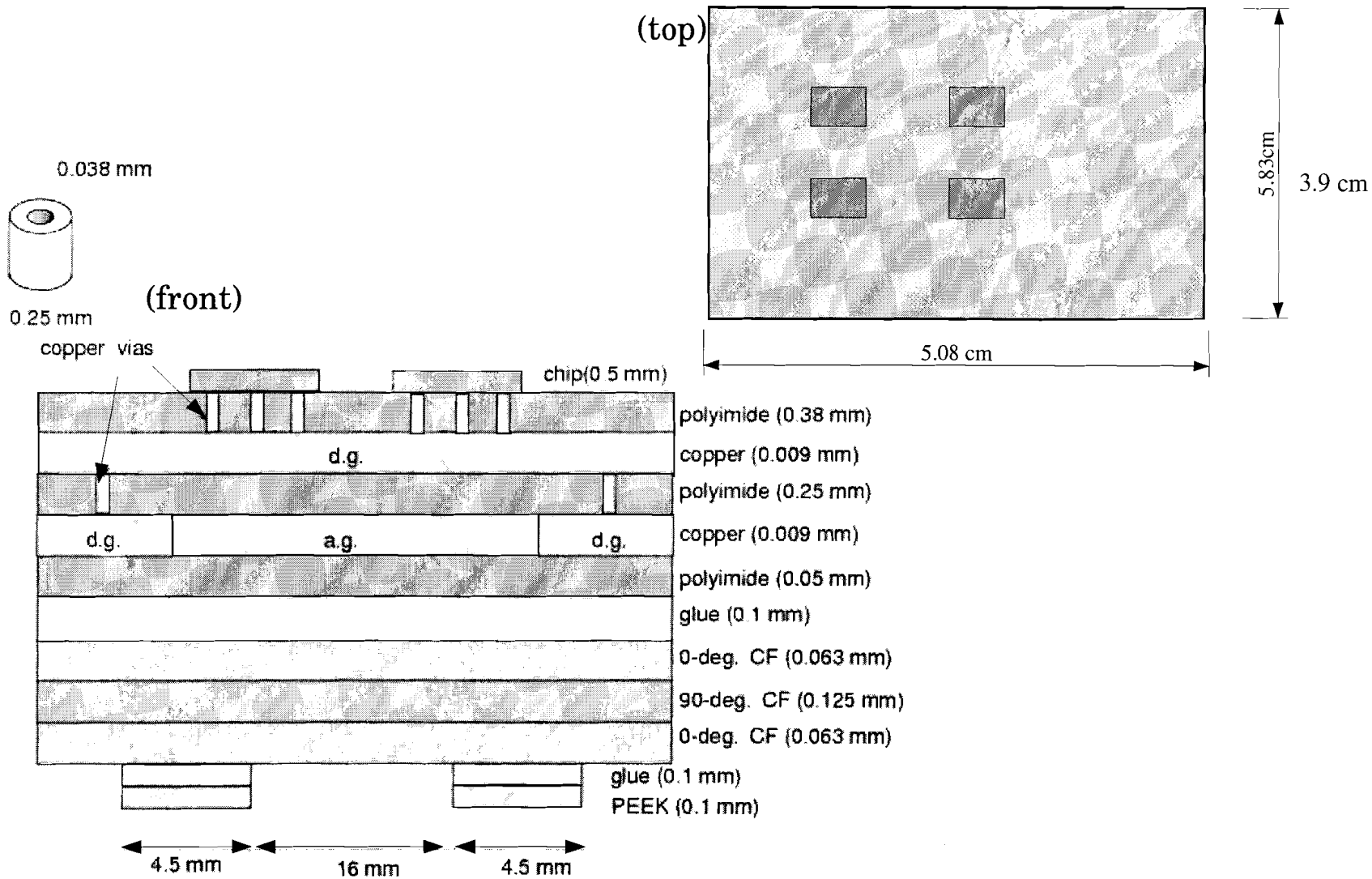
Modified k_gold = (k_gold_pure) * (275 / k_silver_pure)
= 203 (W/m k)

Results

	k_gold (W/m k)	Max. Temp.(C)
Pure	317	5.66
Modified	203	5.83

This effect is small.

Geometry of polyimide miniPC used in this simulation



Maximum temperature of polyimide miniPC,
for different number of vias .

# of vias

Under each chips	Between the copper GNDs	Max.Temp.(C)
4	10	40.59
4	20	40.15
9	10	32.41
9	20	32.36

The number of vias under the chips contributes the temperature, but between the GNDs doesn't.

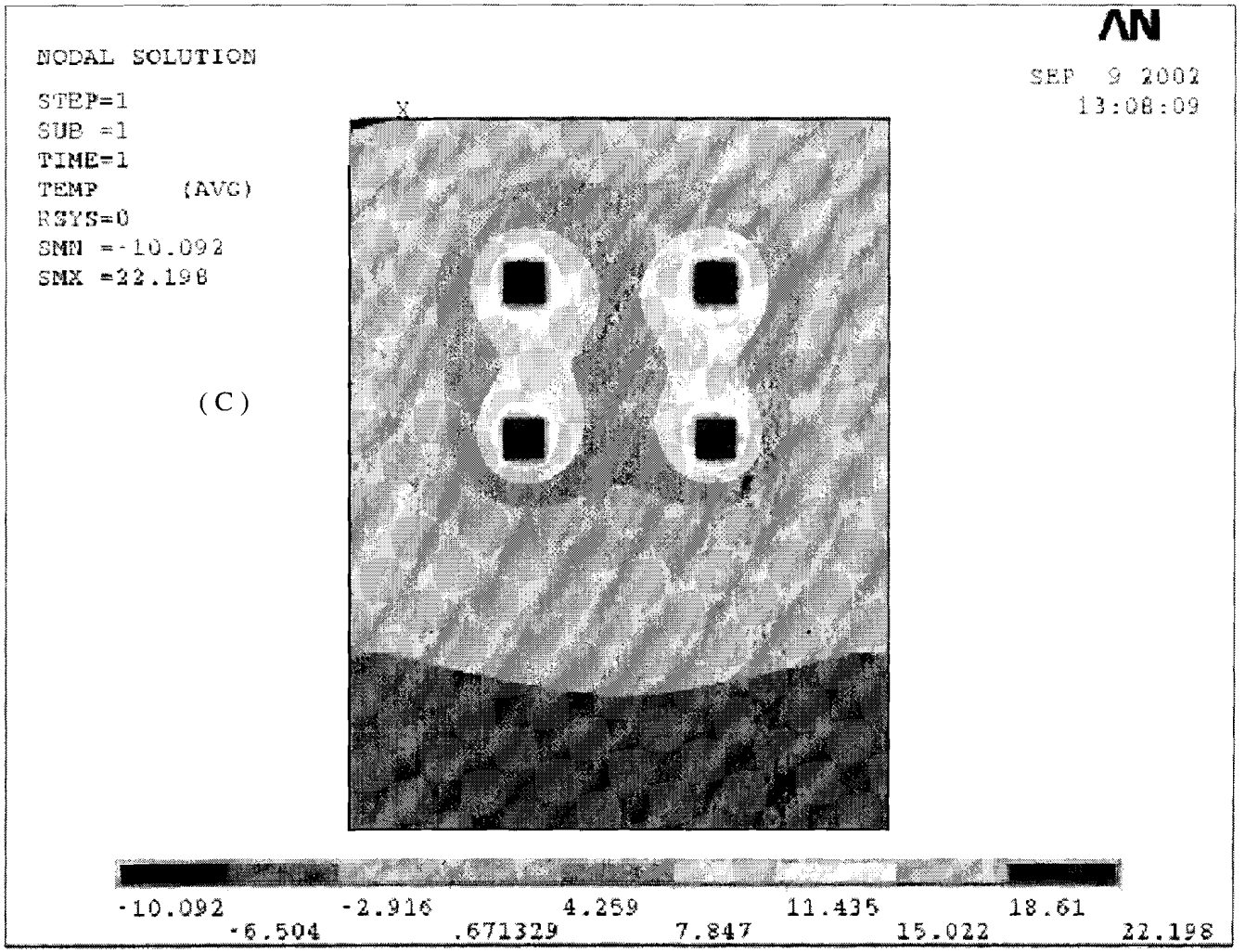
Changing thickness of the copper GNDs

(for polyimide MPC with 9 vias under the chips and 20 between the GNDs.)

	(1)	(2)	(3)	(4)	(5)	(6)
	9 um	9 um	18 um	18 um	27 um	36 um
	9 um	18 um	9 um	18 um	9 um	9 um
Max. Temp.(C)	32.36	31.63	22.57	22.2	18.24	15.74

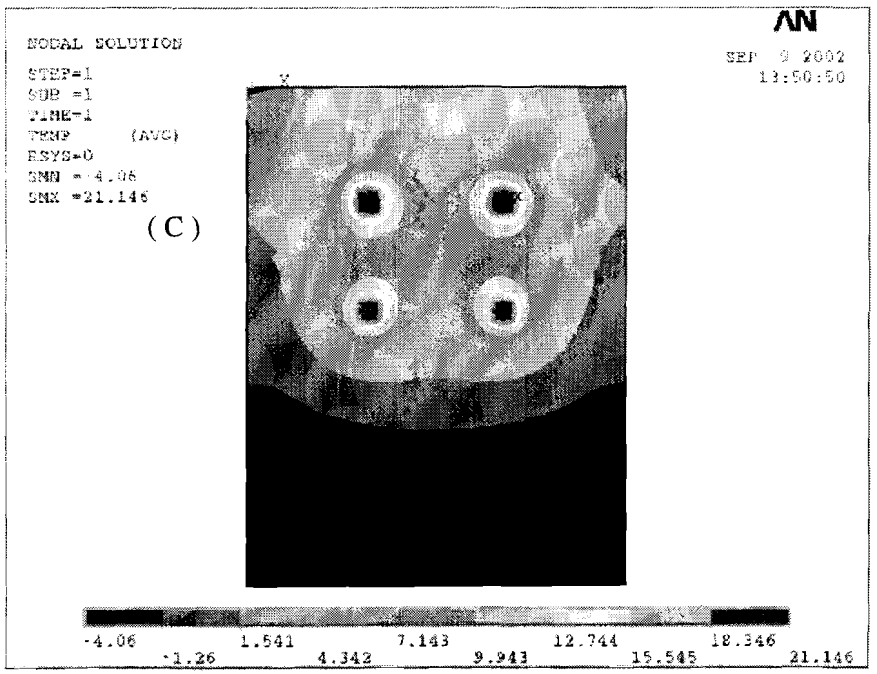
Up-side GND helps cooling down,
but down-side doesn't .

Thermal distribution for the case (4)

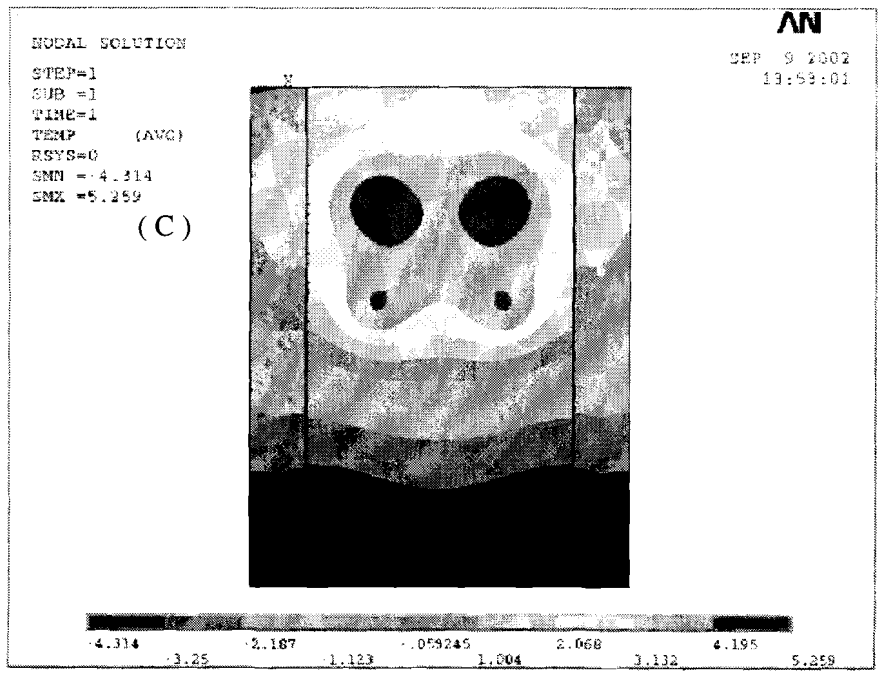


Thermal distribution at the GND layers for the case (4)

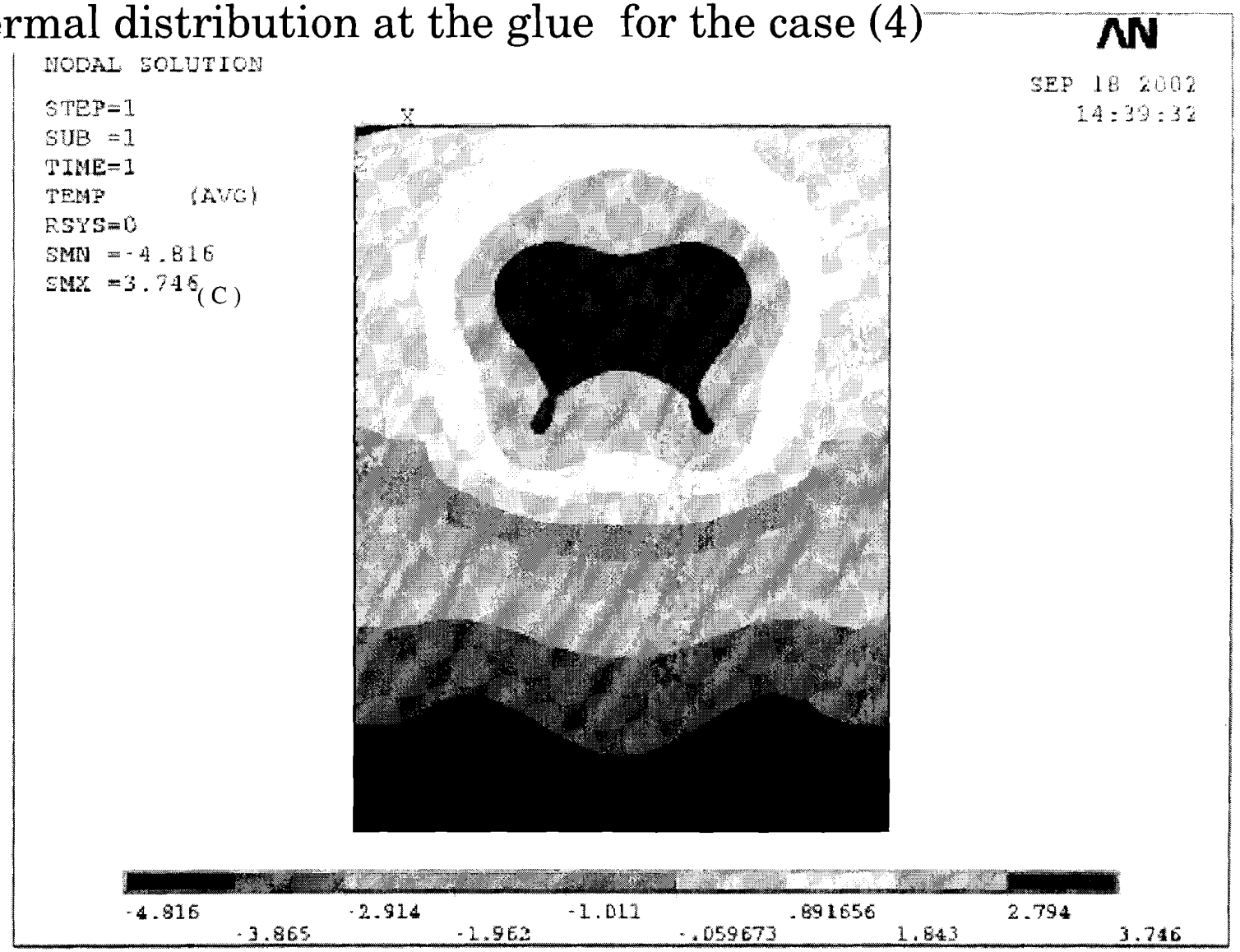
up-side



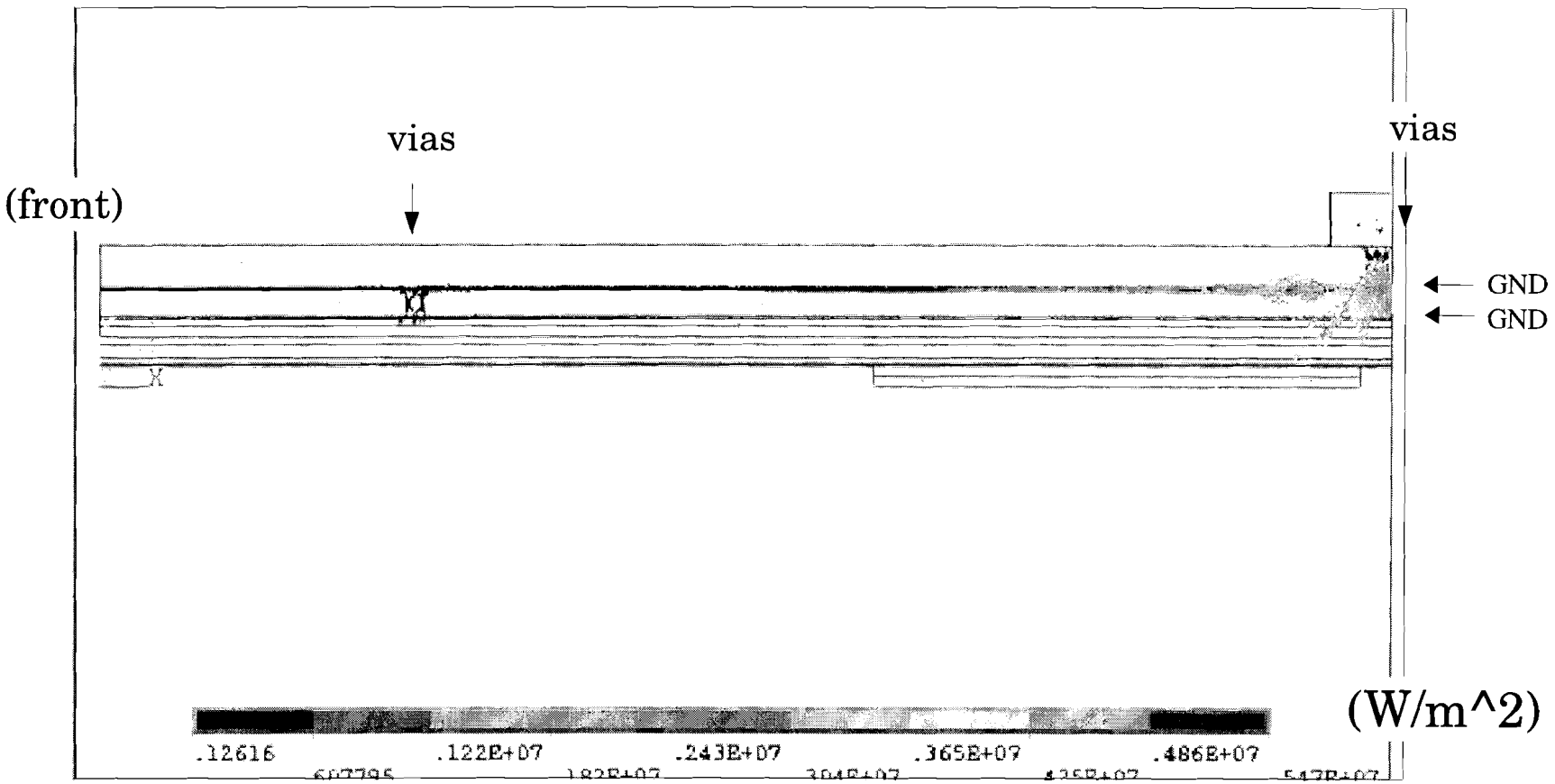
down-side



Thermal distribution at the glue for the case (4)

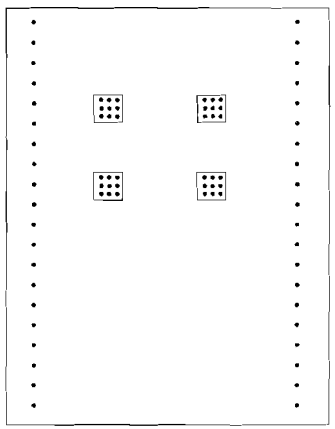


Thermal Flux for the case (4)

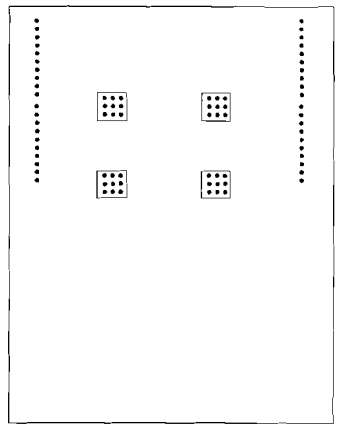


Heat flows mainly through the vias under the chips and then spreads out through the up-side copper GND.

Comparing the temperature of miniPC which have different vias positions (for case (6))



A

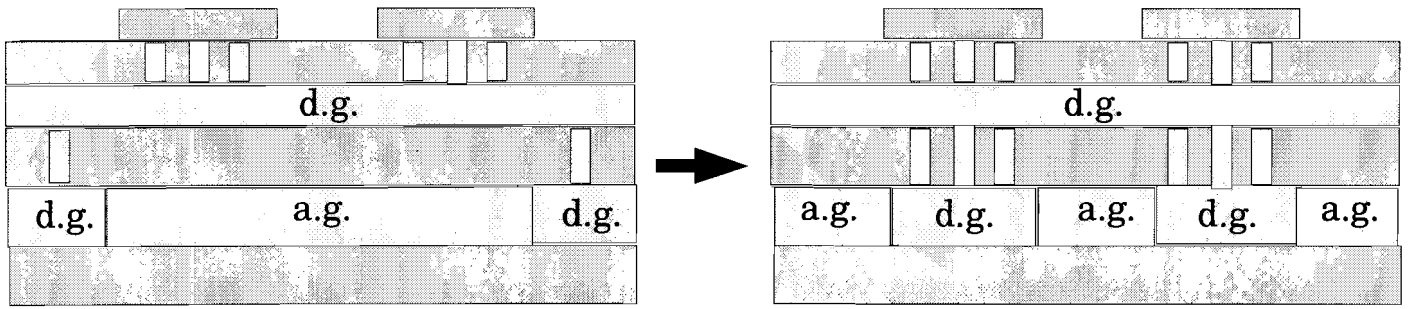


B

	Max. Temp. (C)
A	15.735
B	15.726

Positions of the vias between the GNDs give little contribution to the temperature .

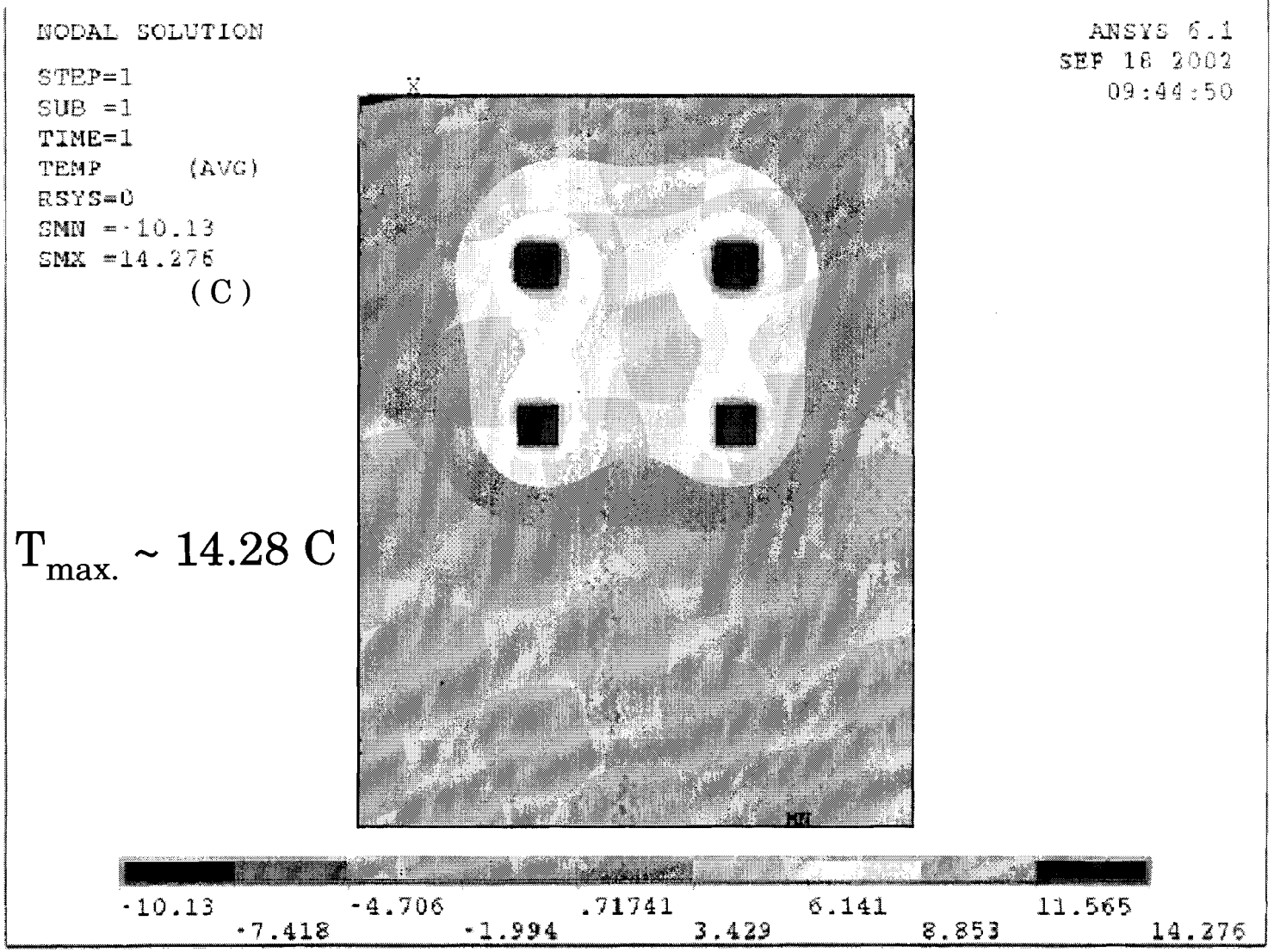
Extending the vias to the "down-side" ground



Not using the side vias, extend the vias under the chips to the "down-side" ground and move the down-side digital ground there.

(thickness of GND = 18 μm)

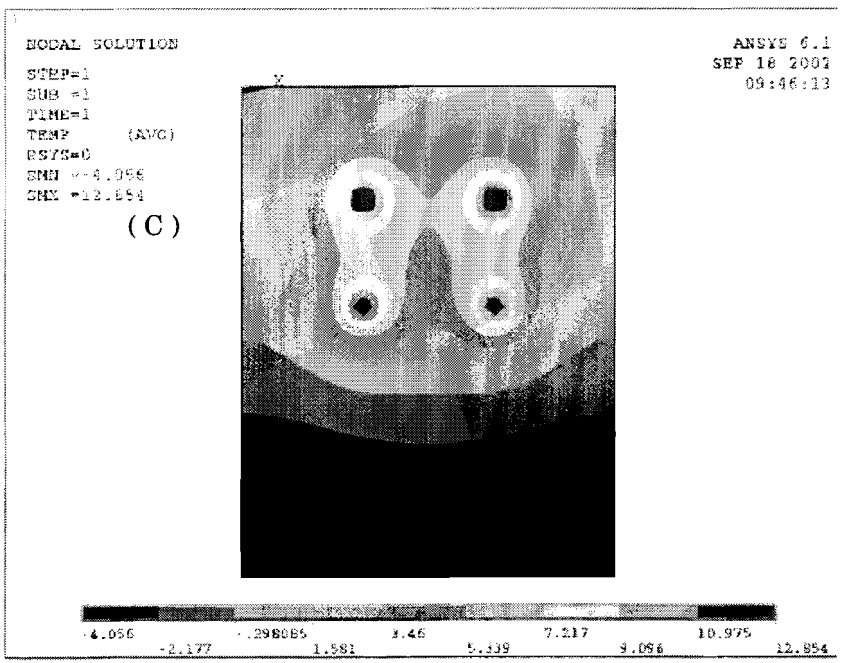
Thermal distribution for 9 vias MPC



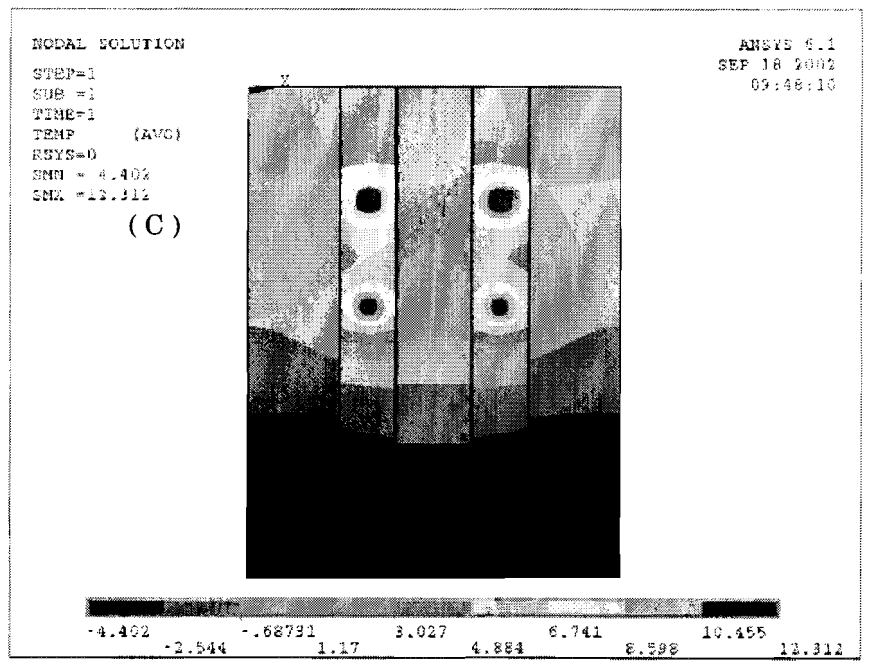
$T_{max.} \sim 14.28$ C

Thermal distribution at the GND layers for 9 vias MPC

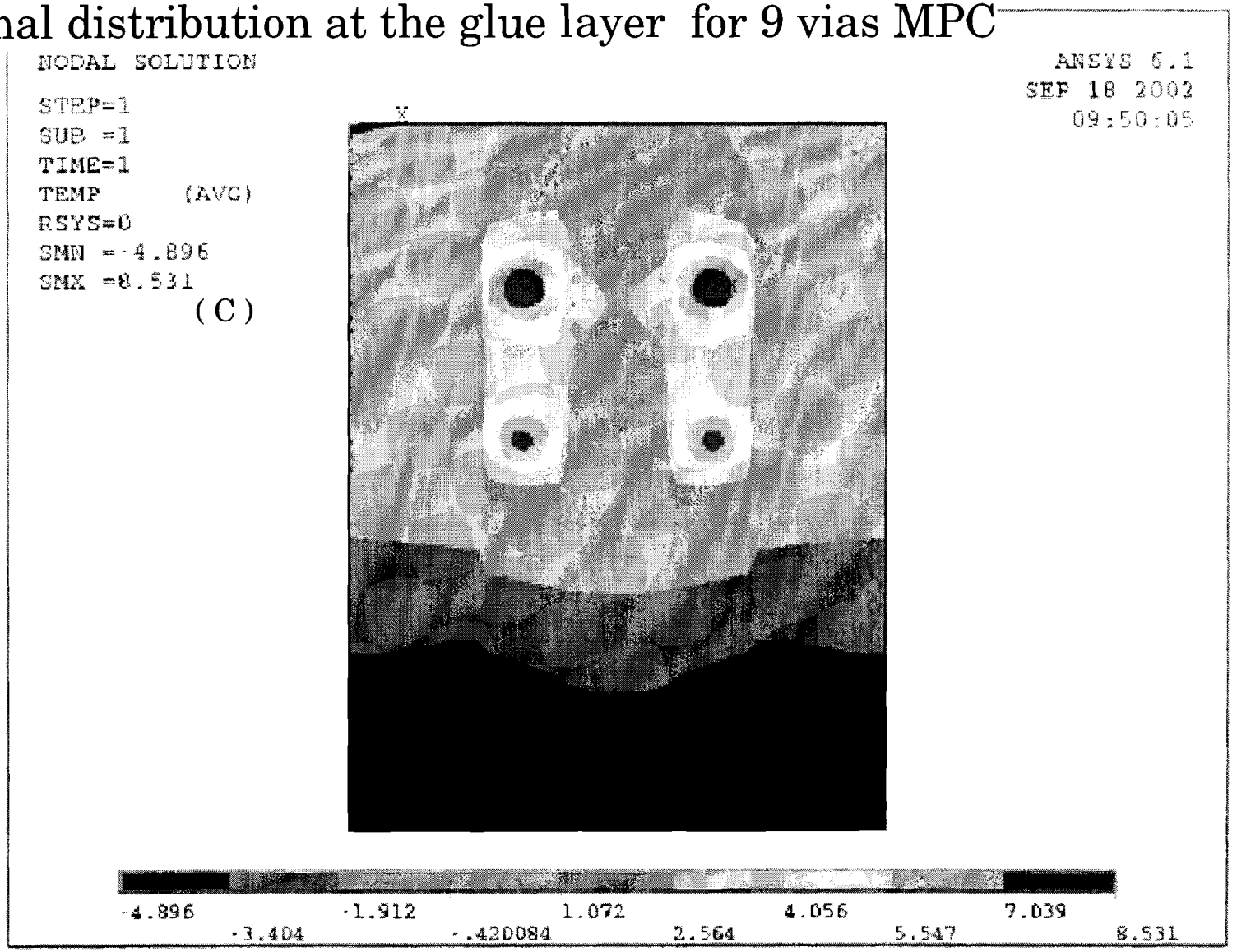
up-side



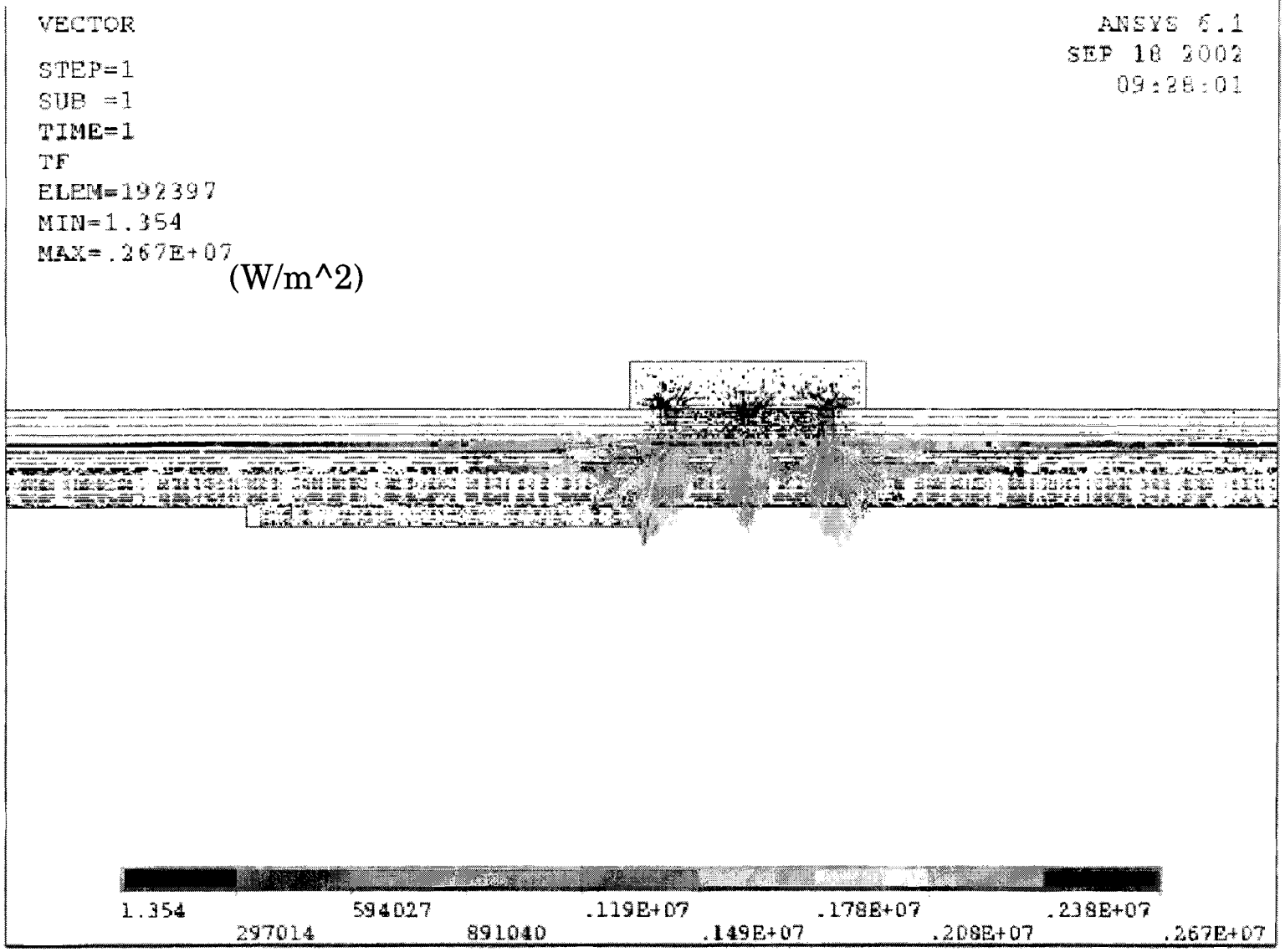
down-side



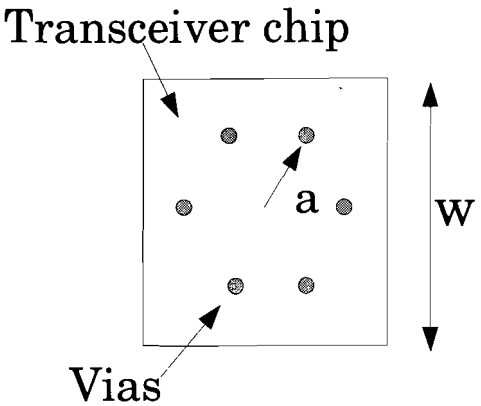
Thermal distribution at the glue layer for 9 vias MPC



Thermal flux for 9 vias MPC

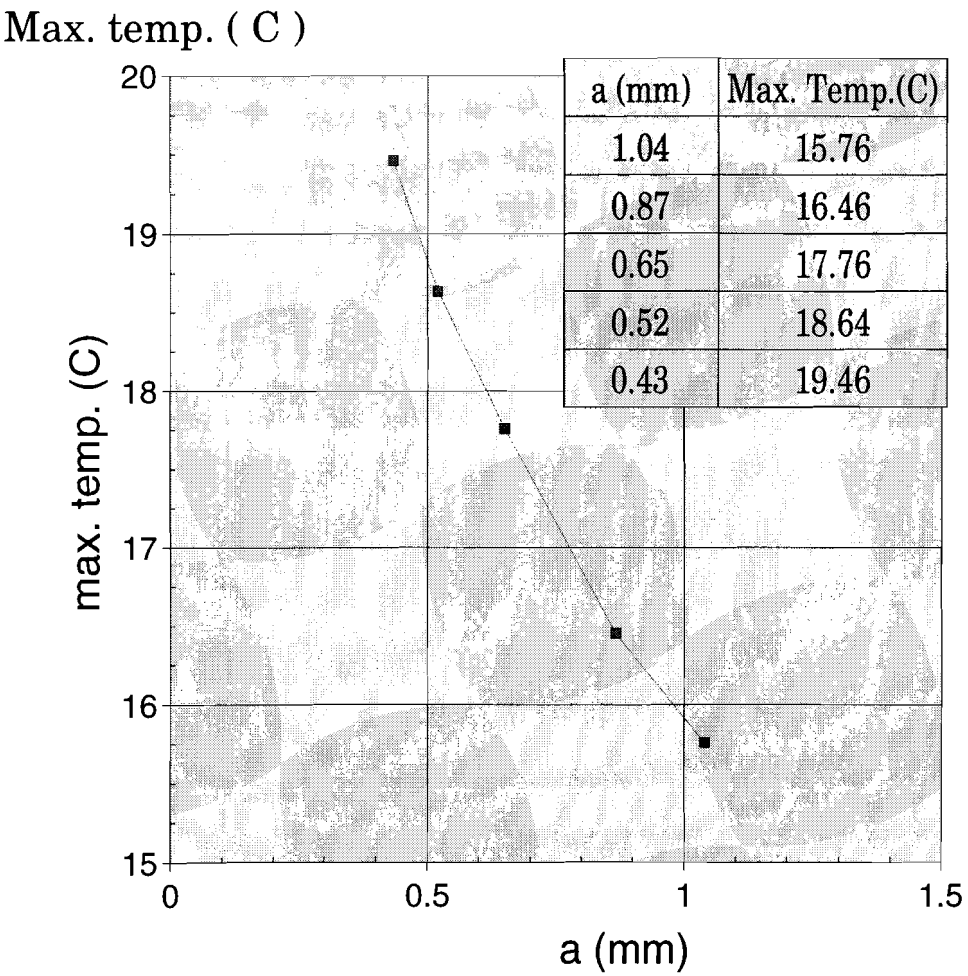


6 vias MPC (Change the number of vias (9 -> 6).)



Positions of the vias

a = w/2.5 , w/3 , w/4 , w/5 , w/6
= 1.04 , 0.87, 0.65, 0.52, 0.43 (mm)

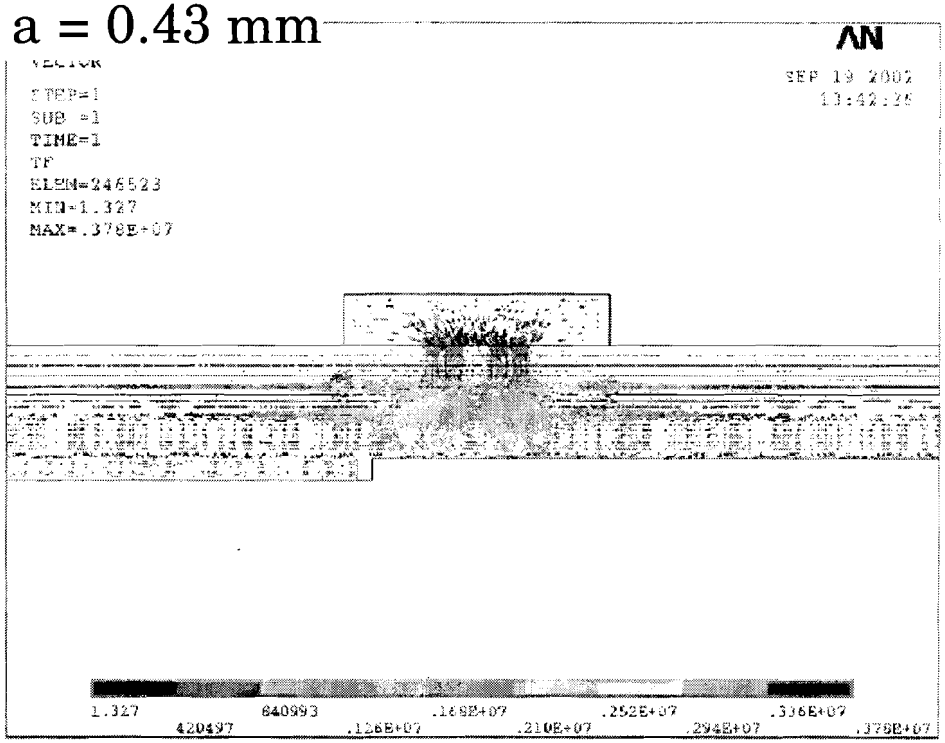


a (mm)	Max. Temp.(C)
1.04	15.76
0.87	16.46
0.65	17.76
0.52	18.64
0.43	19.46

Wide distance between the vias is better.

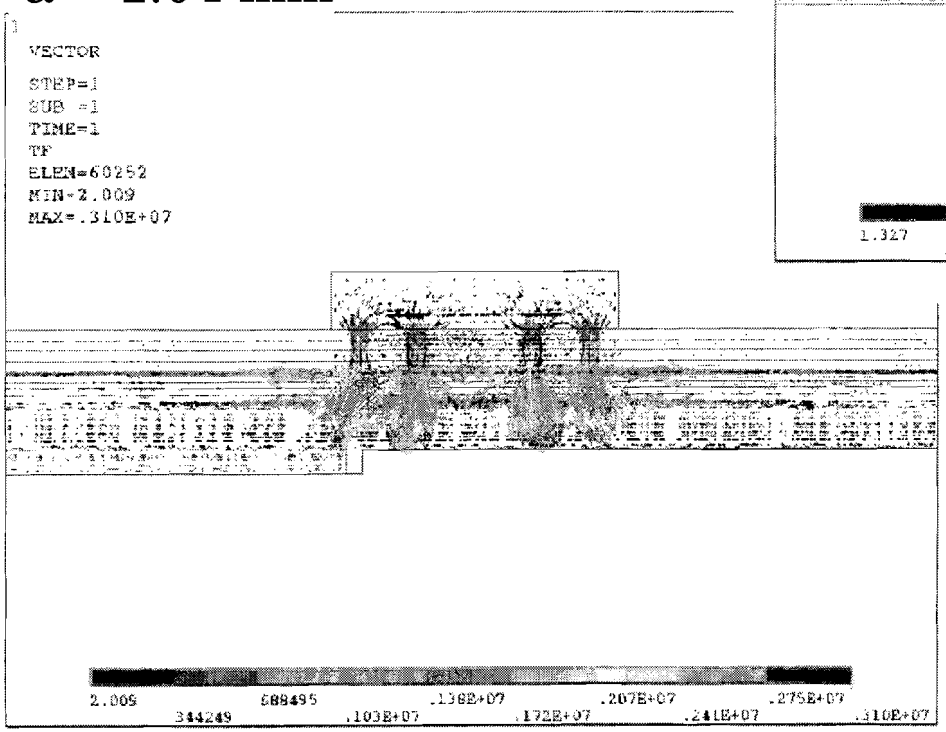
Thermal flux for 6 vias MPC

a = 0.43 mm

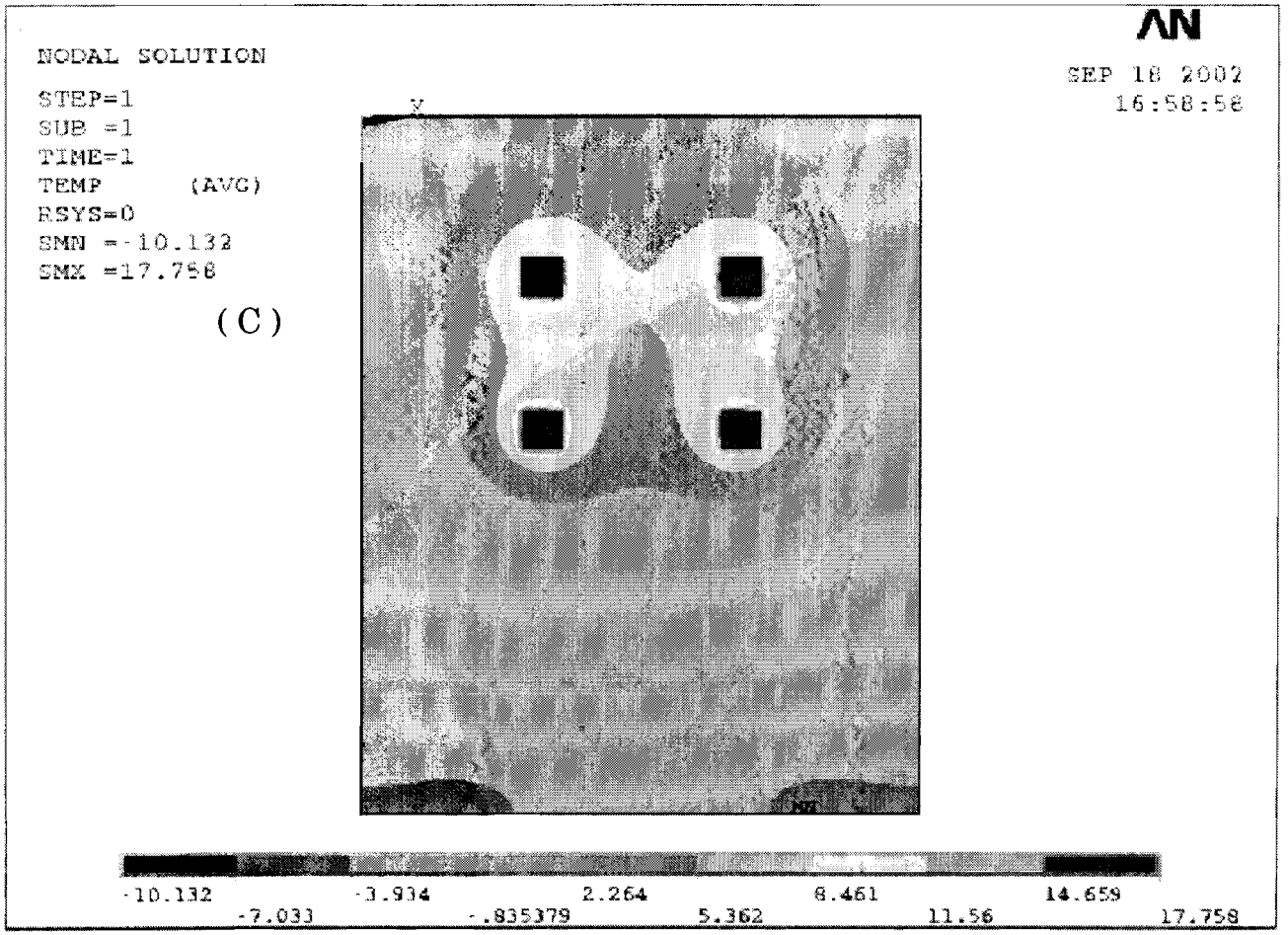


(W/m^2)

a = 1.04 mm

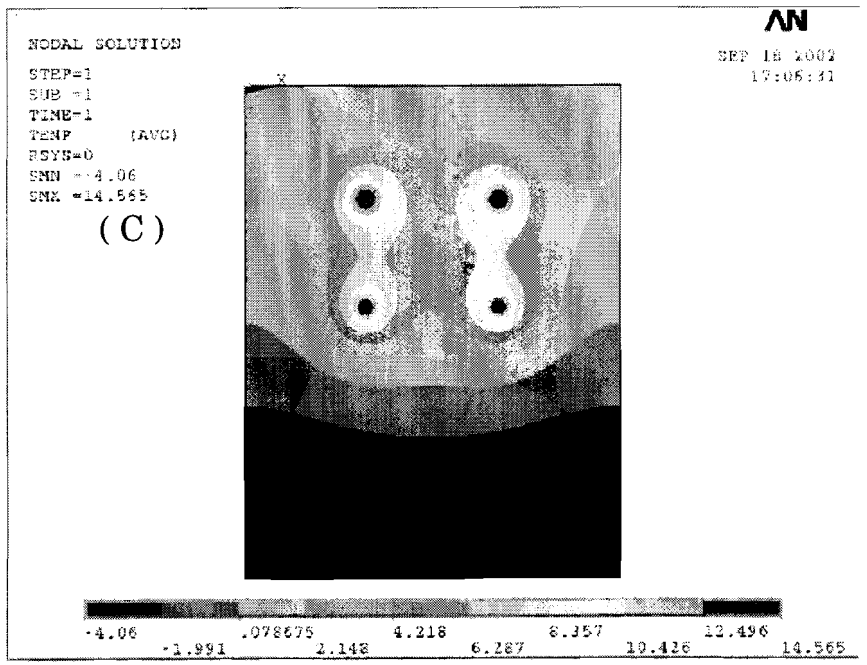


Thermal distribution (for 6 vias MPC : a=0.65mm)

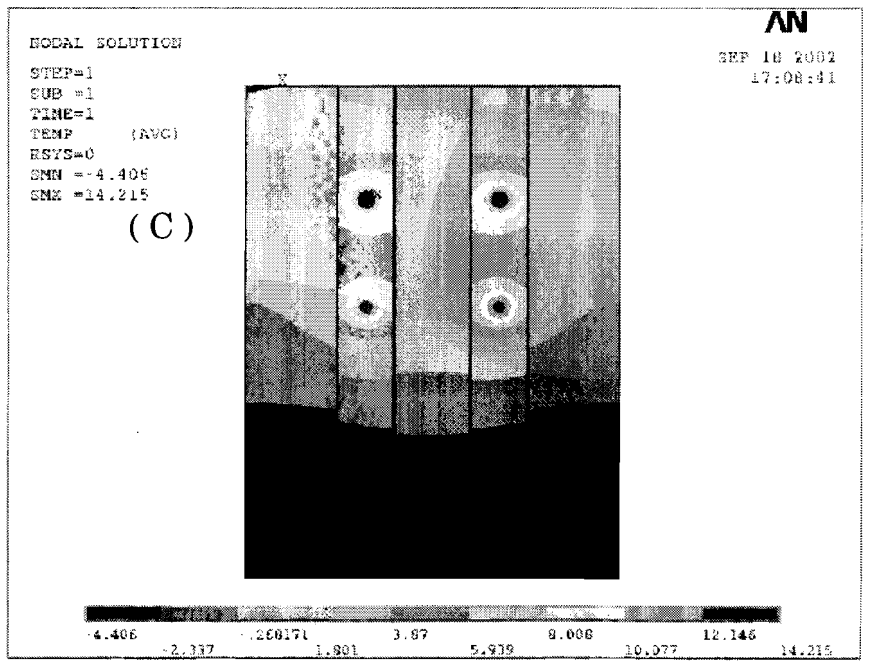


Thermal distribution at the GNDs (for 6 vias MPC : a=0.65 mm)

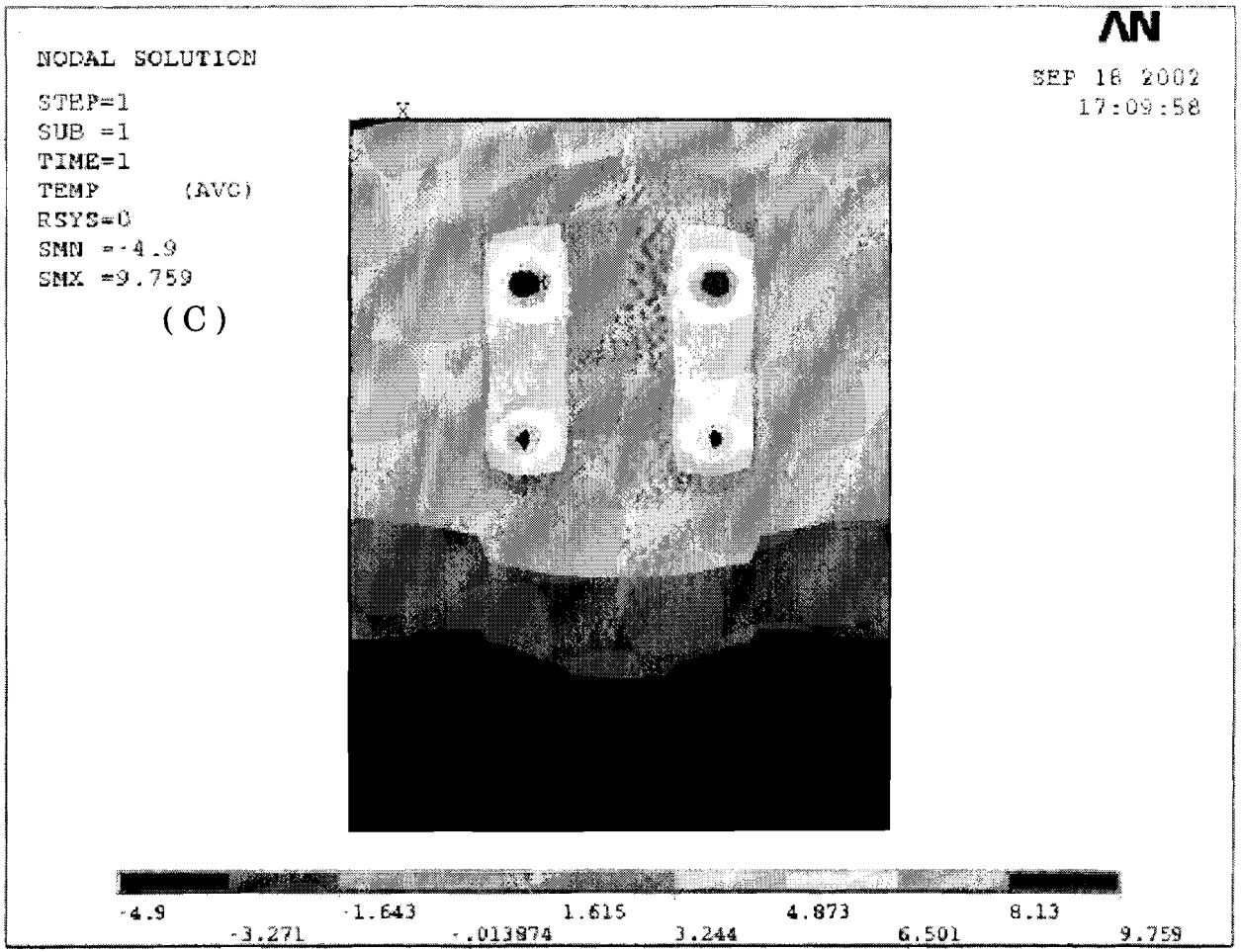
up-side



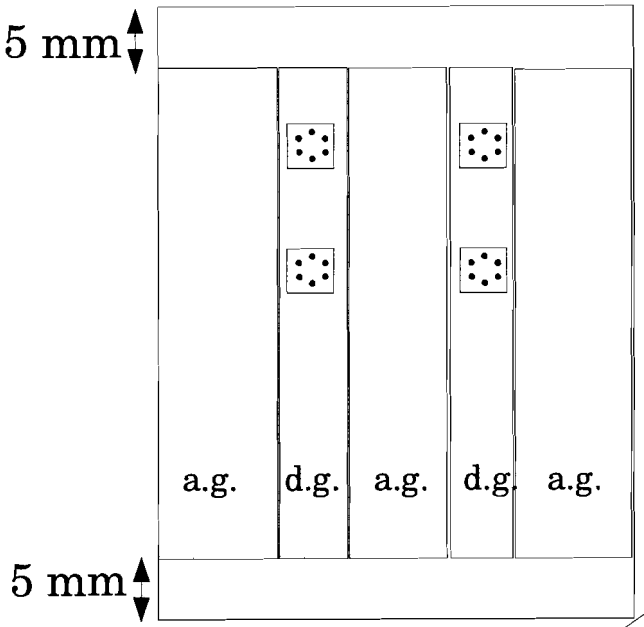
down-side

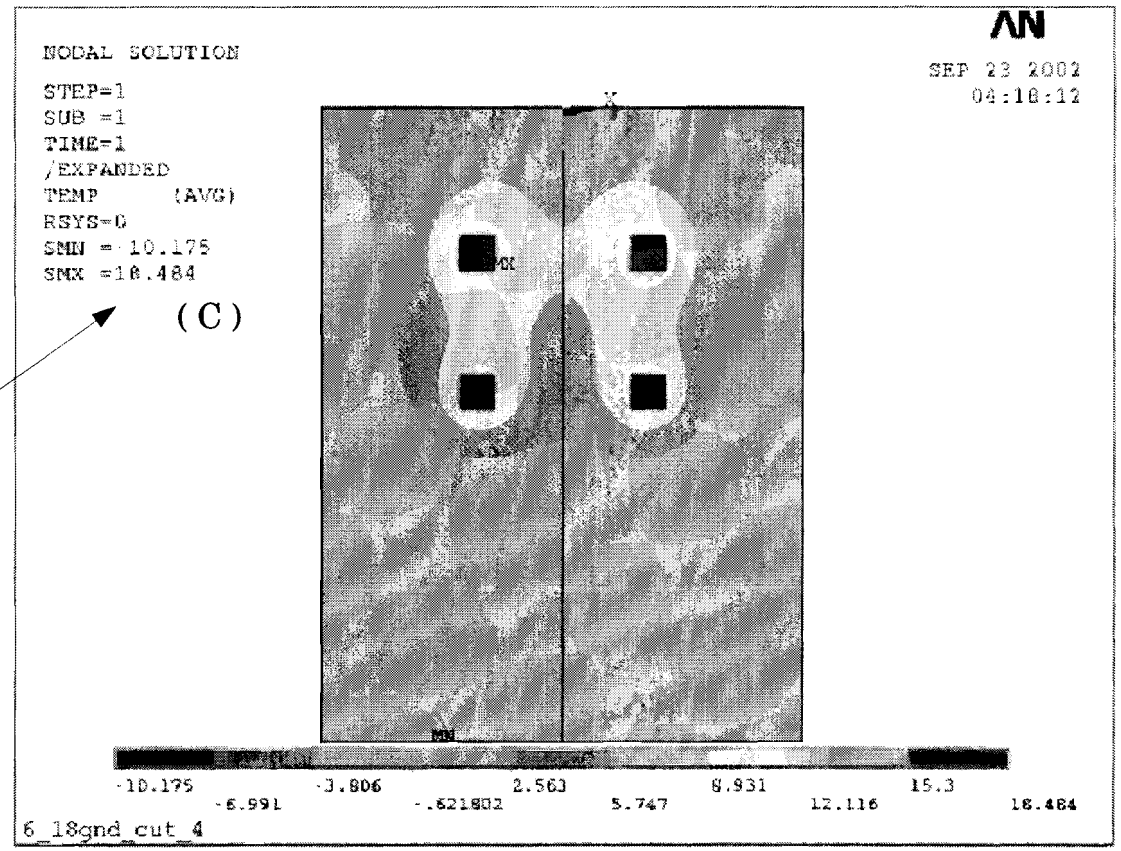


Thermal distribution at the glue layer (for 6 vias MPC : a=0.65 mm)



Cutting the edge of the down-side GNDs (for 6 vias MPC : a=0.65 mm)



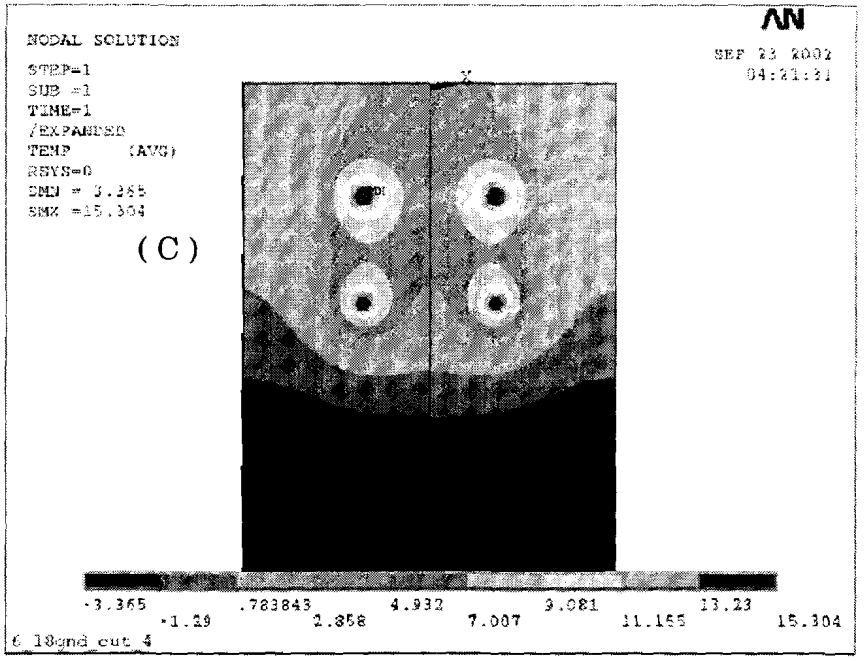


cut : ~18.48 C

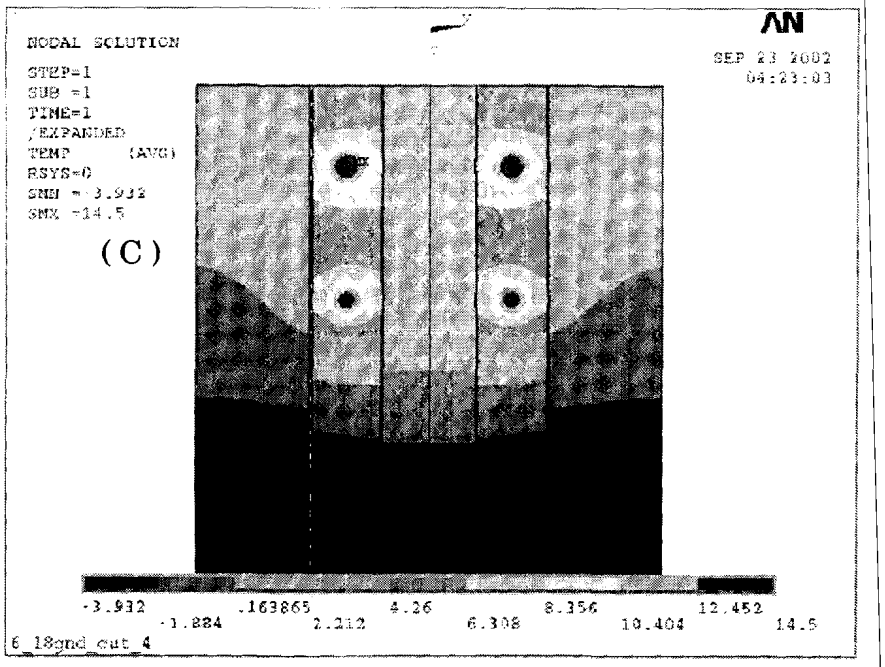
cf) no-cut :~17.76 C

Thermal distribution at the GNDs (for 6 vias MPC : a=0.65 mm)

up-side

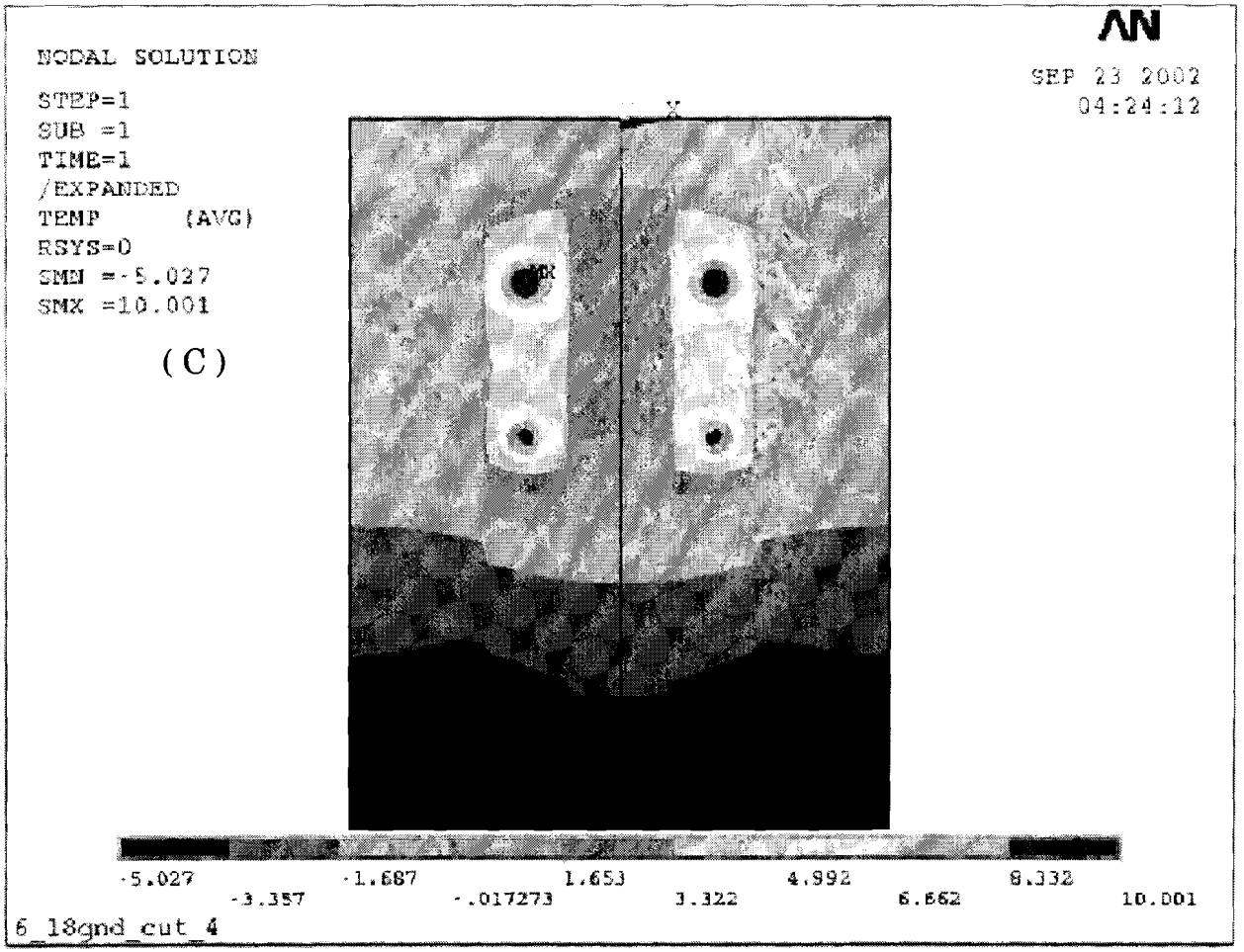


down-side

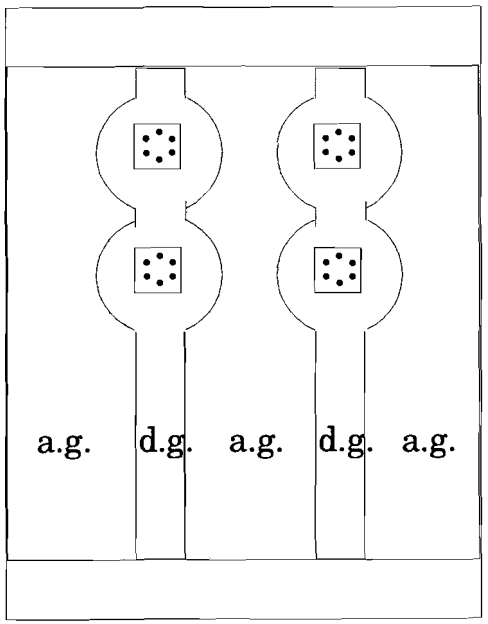


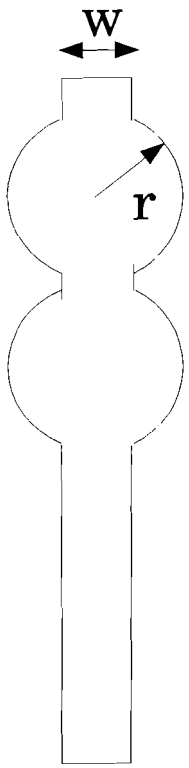
Thermal distribution at the glue layer

(for 6 vias MPC : a=0.65 mm)



Modifying the "down-side" GNDs. (for 6 vias MPC : a=0.65 mm)





Maximum temperature (C)

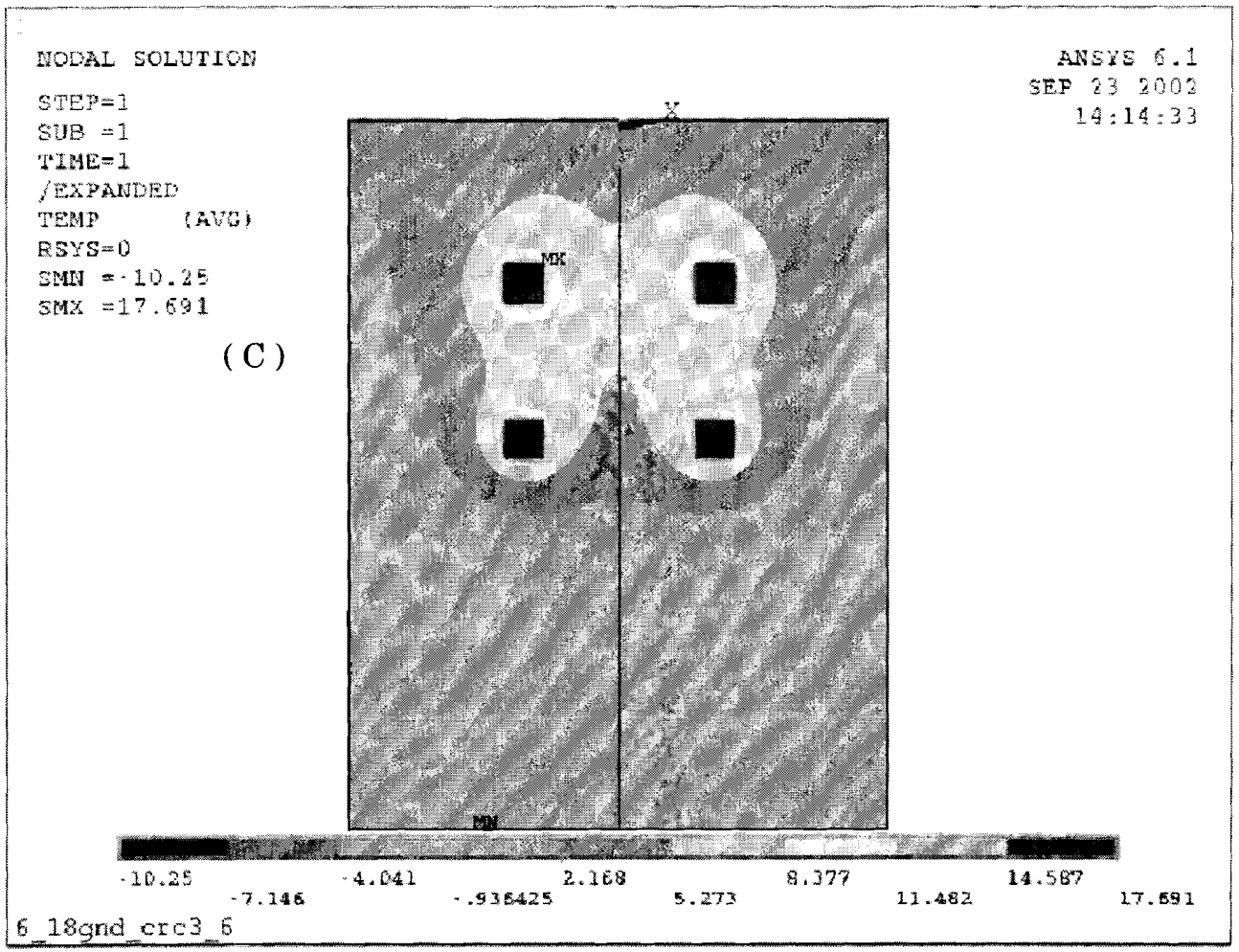
(mm)

w\r	3	4	5	6
3	19.23	18.57	18.07	17.69
4	19.00	18.40	18.02	17.71
5	18.71	18.32	18.01	17.71
6	18.37	18.23	17.96	17.71

cf) not modified : ~18.48 C

Thermal distribution

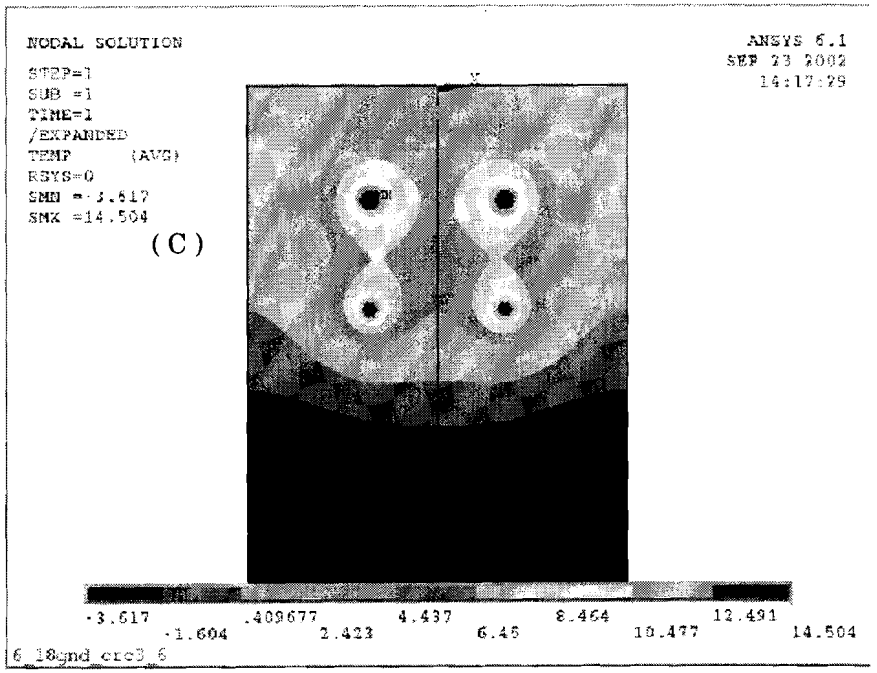
(for 6 vias MPC : a=0.65 mm : w\r = 3mm\6mm)



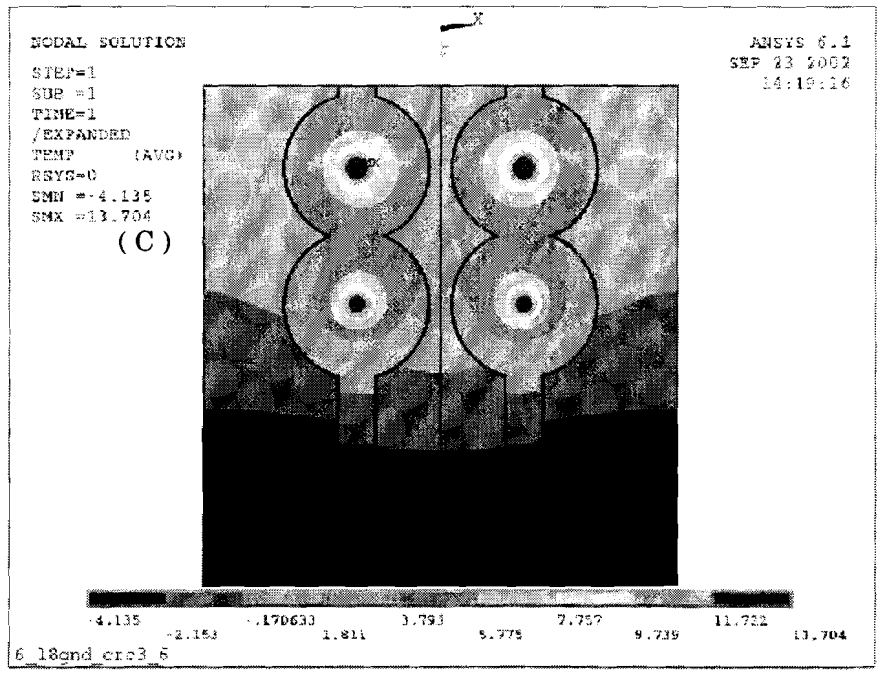
Thermal distribution at the GND layers

(for 6 vias MPC : a=0.65 mm : w\r = 3mm\6mm)

up-side

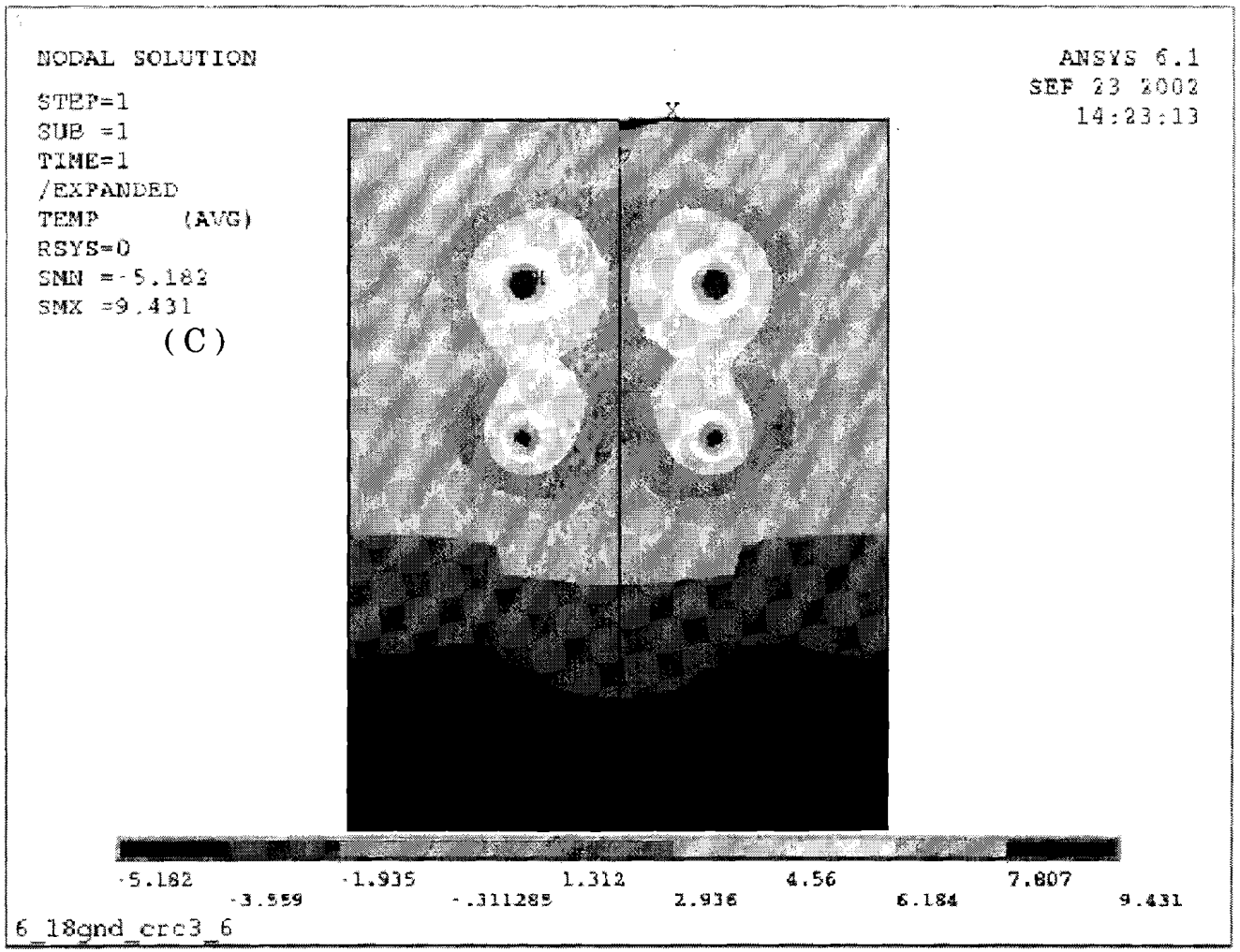


down-side



Termal distribution at the glue layer

(for 6 vias MPC : a=0.65 mm : w\r = 3mm\6mm)



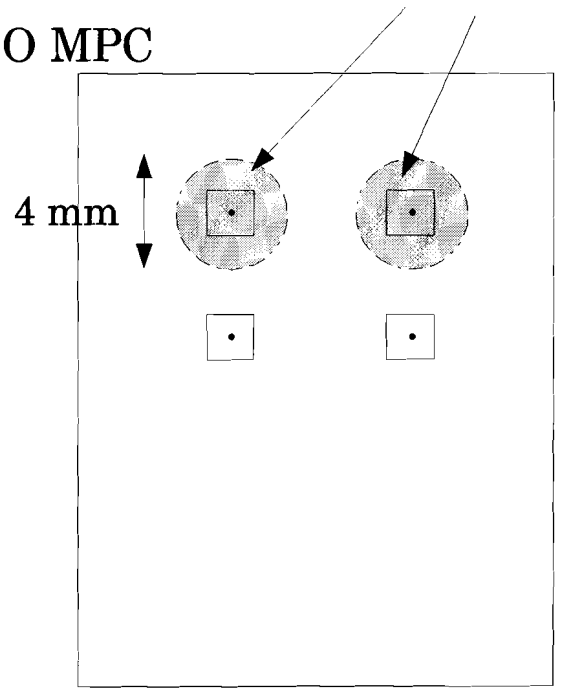
Air in the glue

for BeO and polyimide MPC(w/r=3/6)

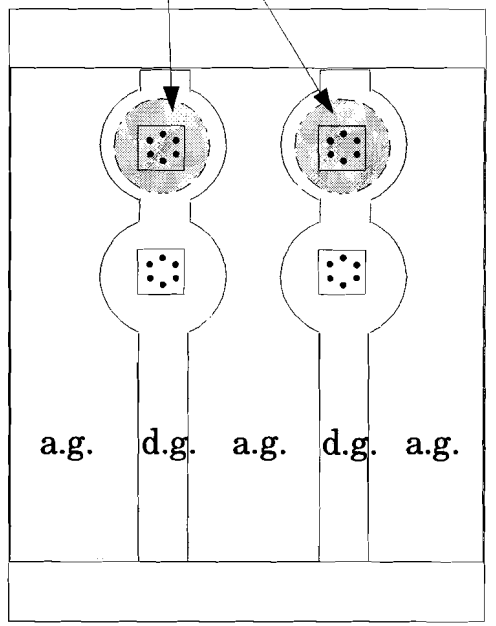
Remove the epoxy in this area and replace it with air

(k_{air} = 0.023 W/m-K)

BeO MPC



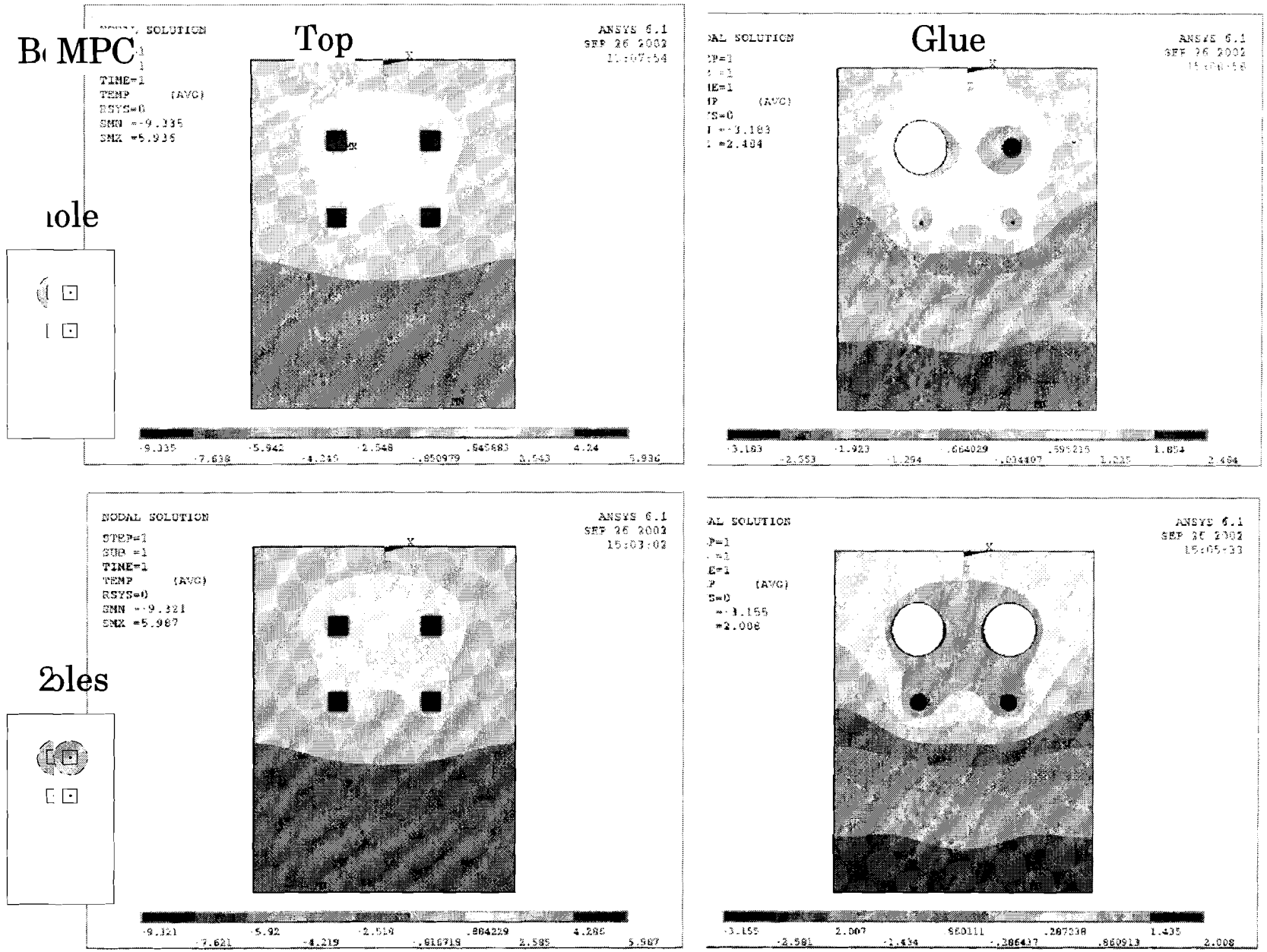
Polyimide MPC



Result

	BeO	Polyimide
normal	5.66	17.69
1 hole	5.94	19.71
2 holes	5.99	19.87

(C)


B MPC
Top
Glue
ole
2bles
NODAL SOLUTION
STEP=1
SUB =1
TIME=1
TEMP (AVG)
RSYS=0
SMN =-9.335
SMX =5.936
ANSYS 6.1
SEP 26 2002
15:07:54
-9.335
-7.638
-5.942
-4.245
-2.548
-.850979
.845883
2.543
4.24
5.936
-3.183
-2.553
-1.923
-1.294
-.664029
-.034407
.595215
1.225
1.854
2.484
NODAL SOLUTION
STEP=1
SUB =1
TIME=1
TEMP (AVG)
RSYS=0
SMN =-9.321
SMX =5.987
ANSYS 6.1
SEP 26 2002
15:03:02
-9.321
-7.621
-5.92
-4.219
-2.518
-.816719
.884229
2.585
4.286
5.987
-3.155
-2.581
2.007
-1.434
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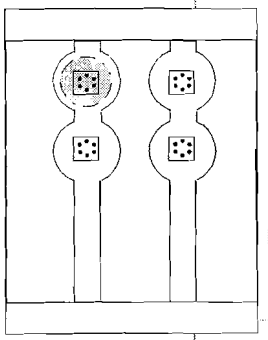
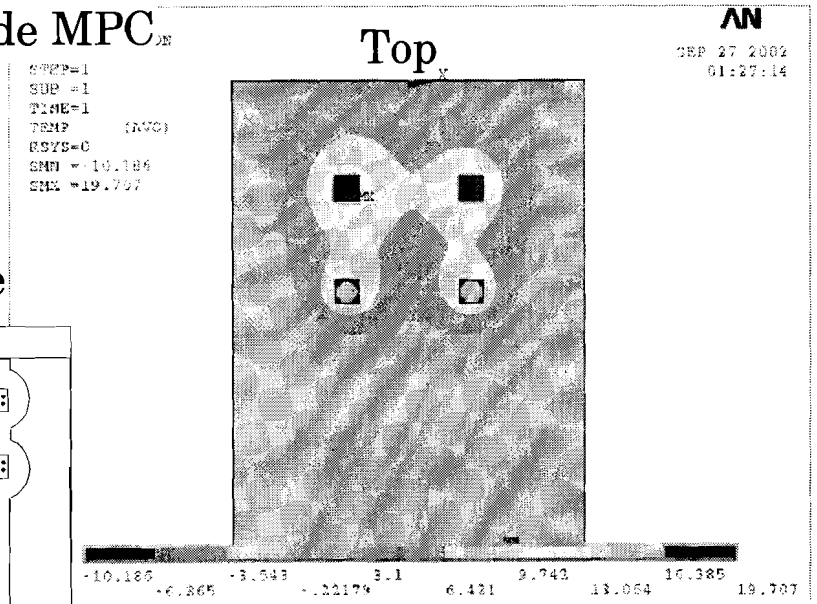
-.286437
.287238
.860913
1.435
2.008

Polyimide MPC

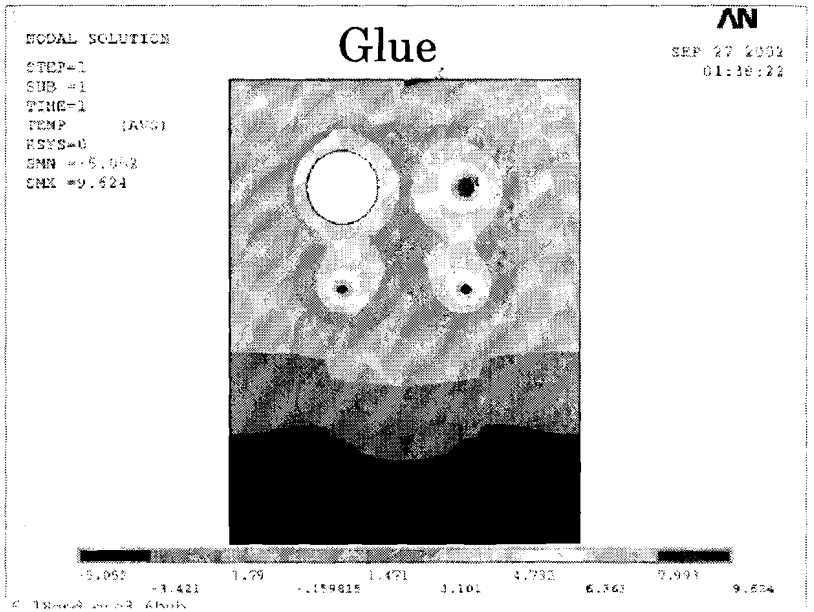
1 hole



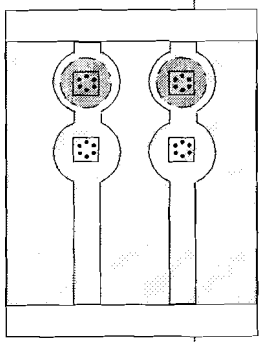
Top

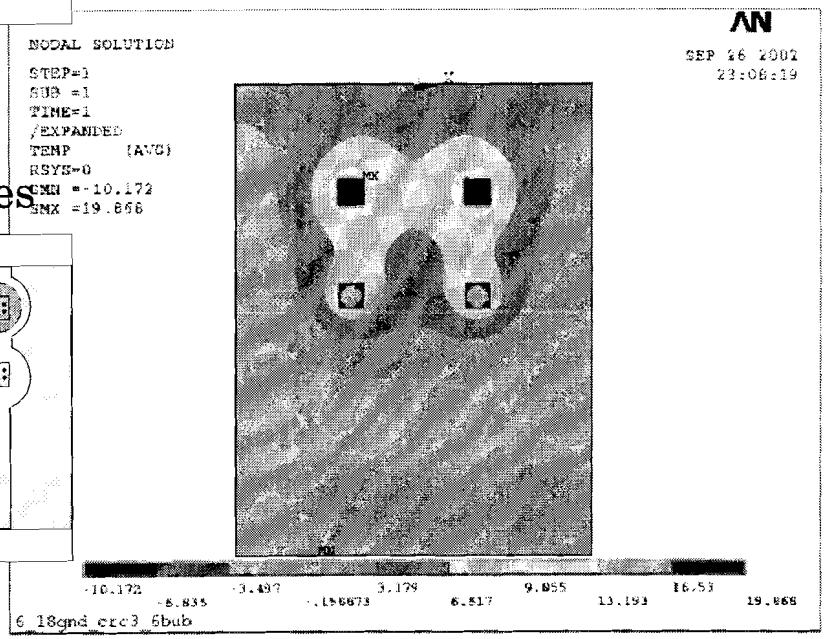


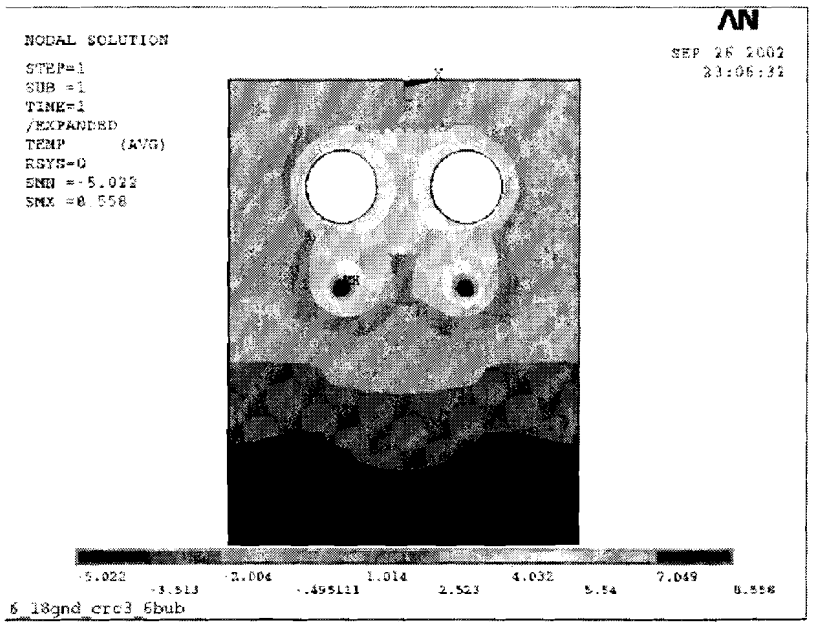
Glue



2 holes

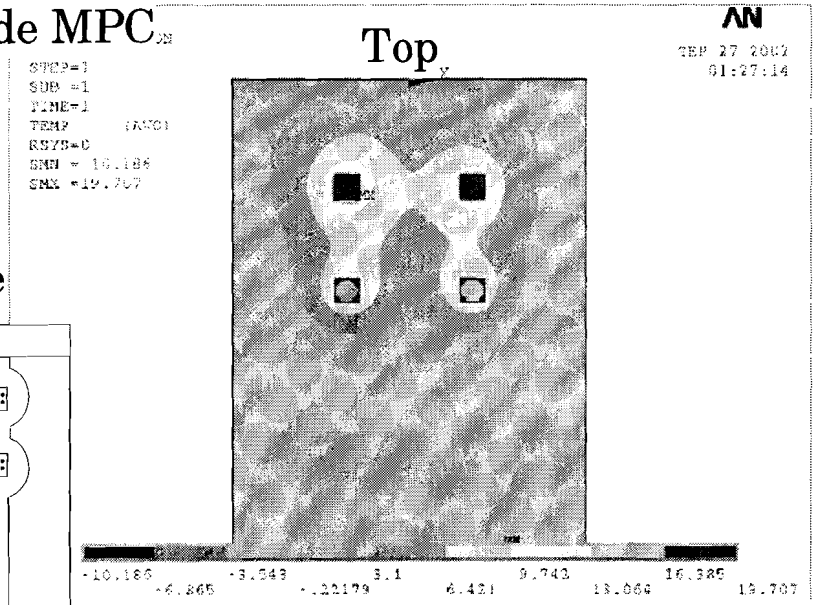




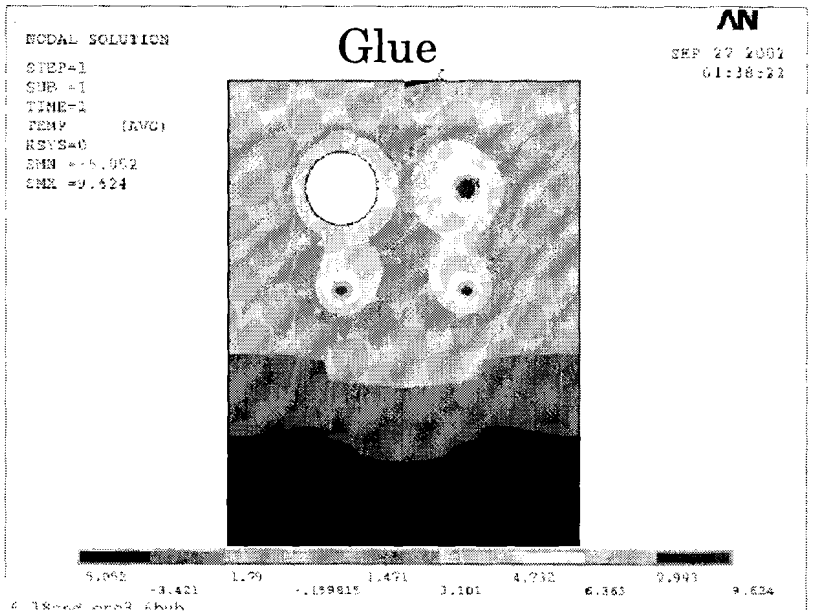


Polyimide MPC

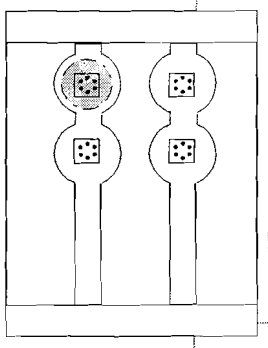
Top



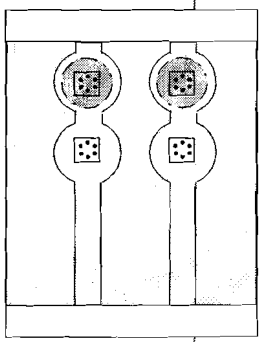
Glue

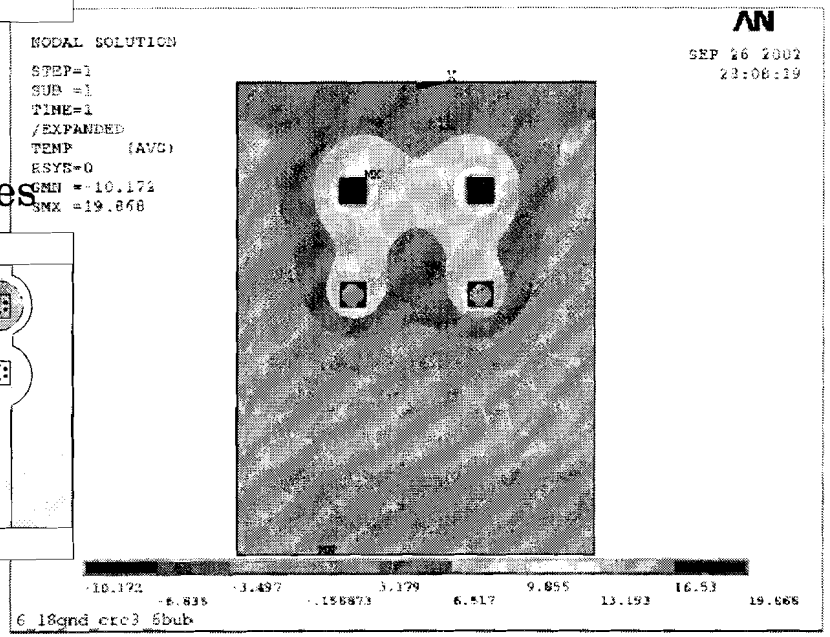


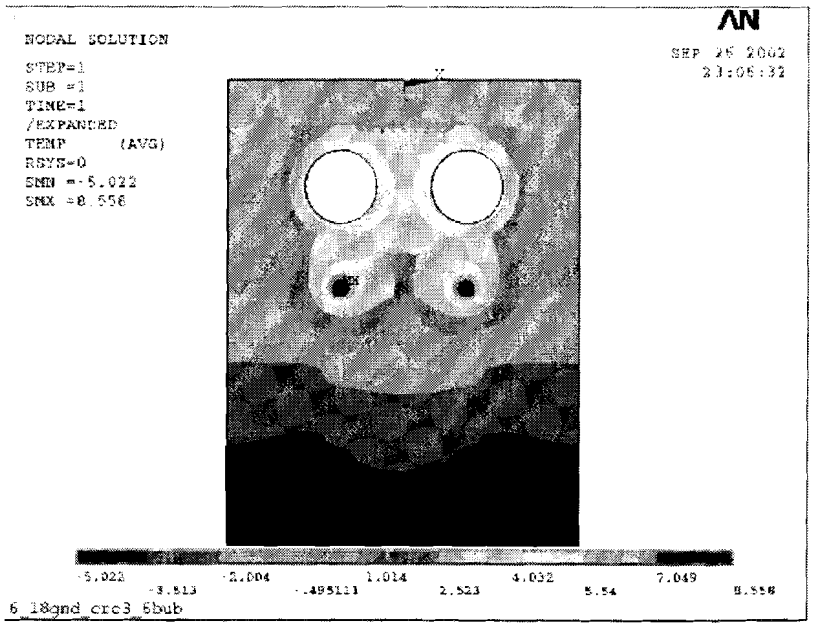
1 hole



2 holes





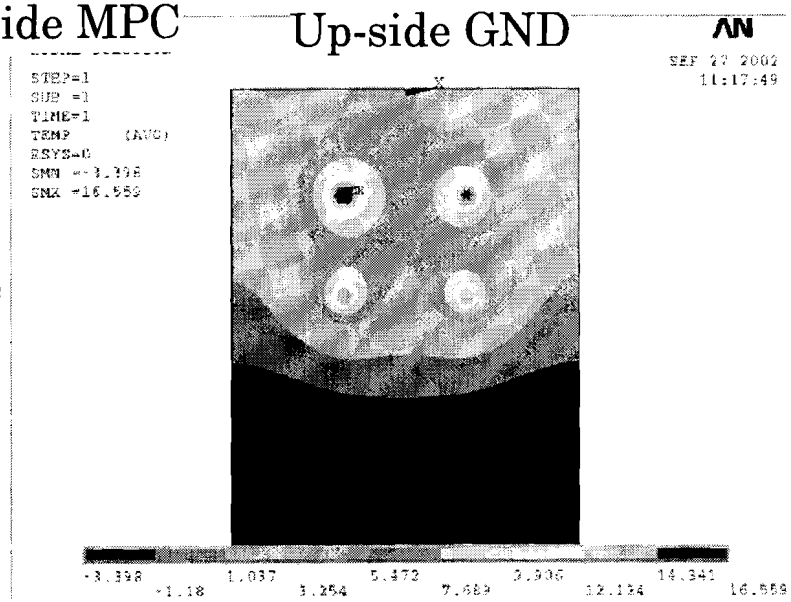


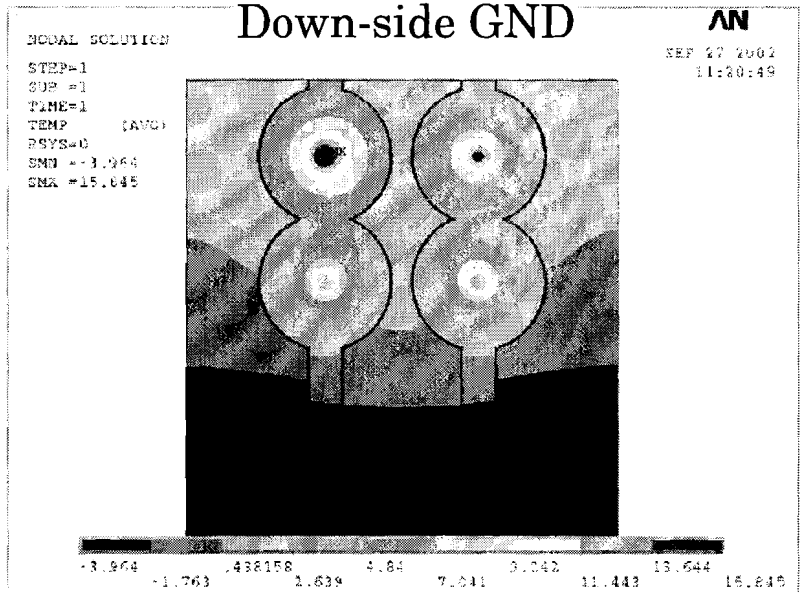
Polyimide MPC

Up-side GND

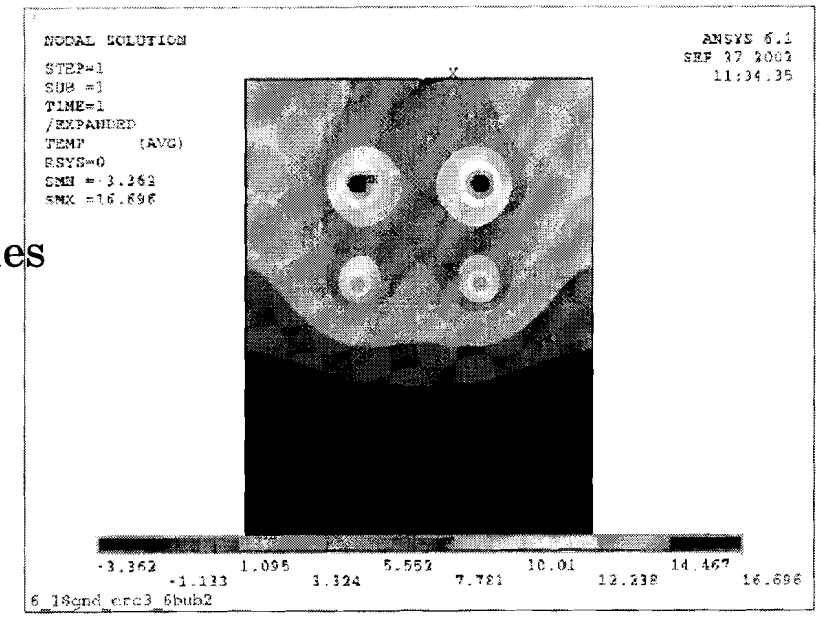
Down-side GND

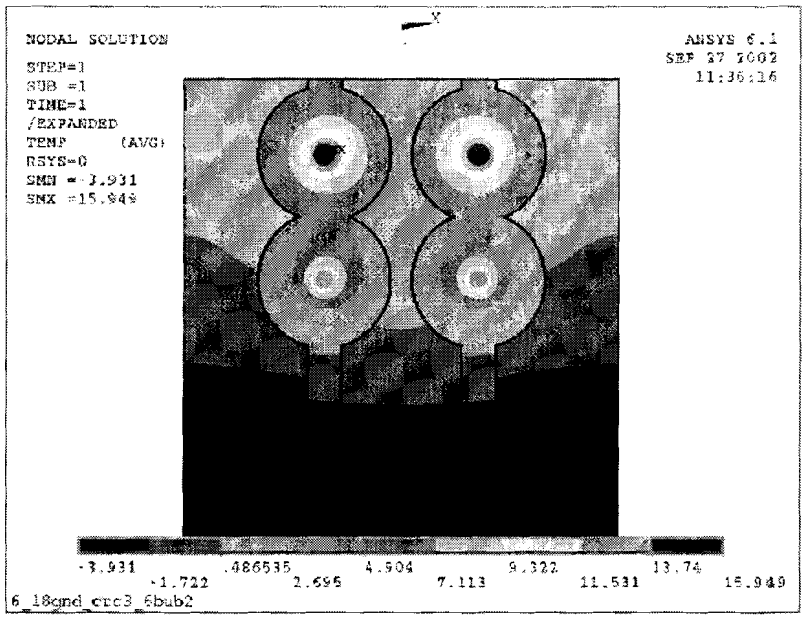
1 hole





2 holes



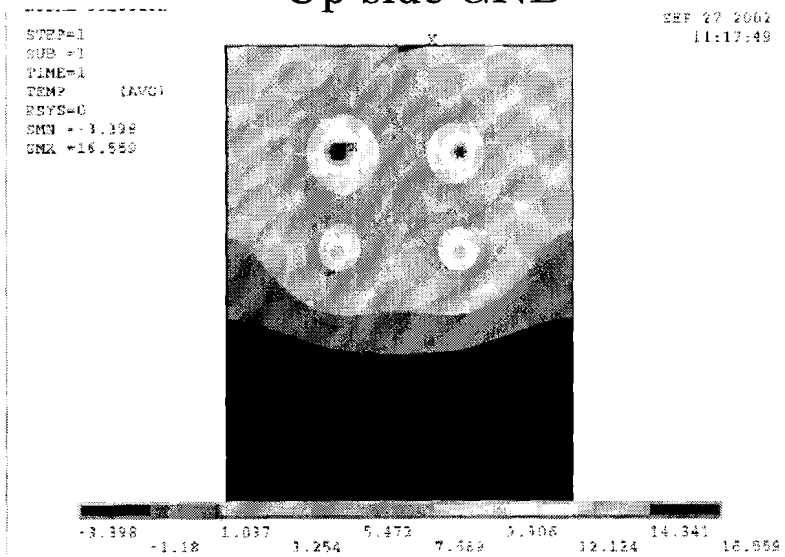


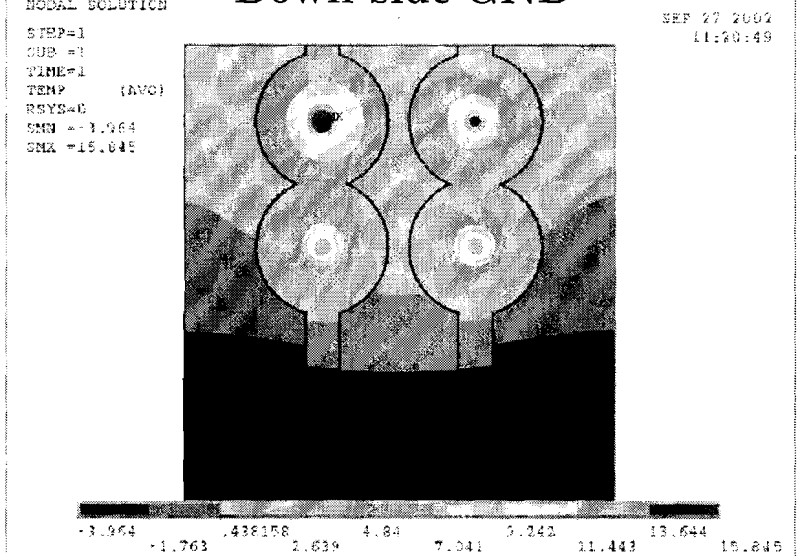
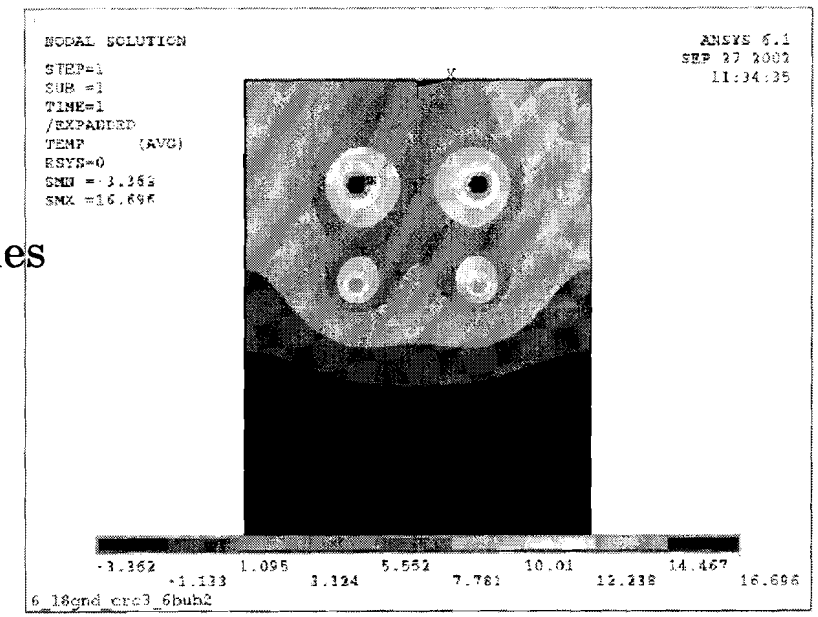
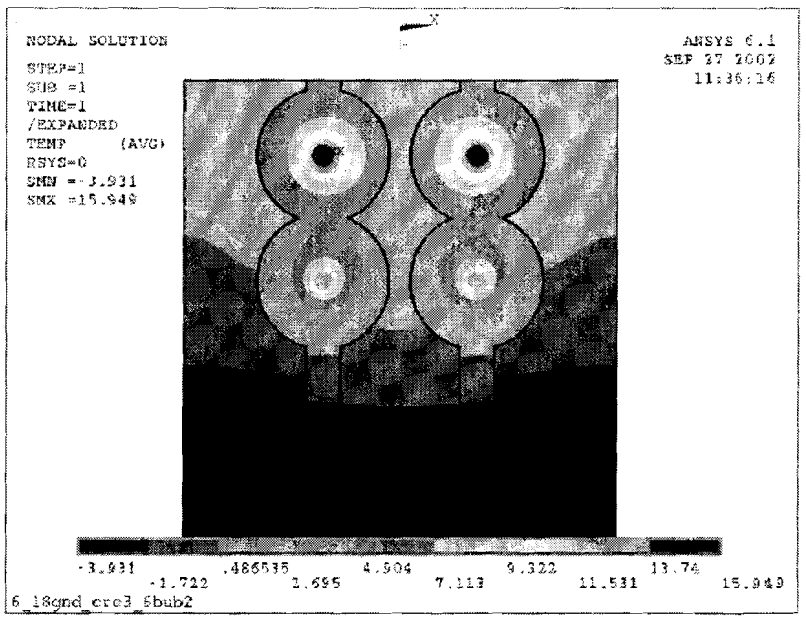
Polyimide MPC

Up-side GND

Down-side GND

1 hole





2 holes